EUROPEAN EDITION

# EDN®

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

MAY 11, 1995

PCX104 bus ruggedizes PC104 pg 15

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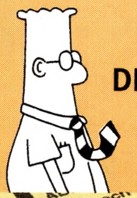

## EDN'S 1995 DSP-CHIP DIRECTORY PG 40

## SPECIAL EXPANDED DESIGN IDEAS SECTION PG 129

A CAHNERS PUBLICATION

#0008008112/20020# (9509 ) 960
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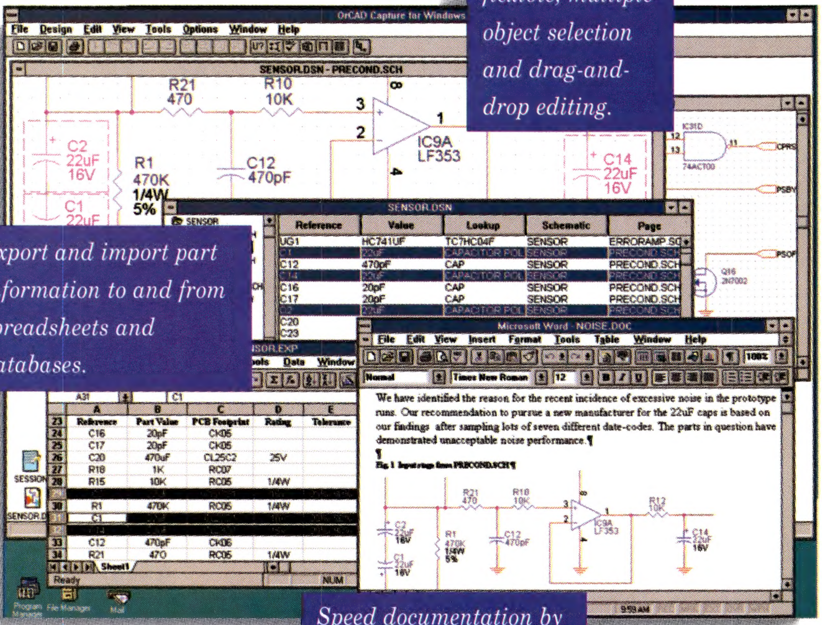
12 JUL 1995

# It Cuts, Pastes, Drags, Drops, Imports, Exports & Makes Schematic Capture Click.



SENSOR.DSN

| Reference | Value | Lookup | Schematic | Page |
|---|---|---|---|---|
| UG1 | HC741UF | TC7HC04F | SENSOR | ERRORAMP.SC |
| C1 | 22uF | CAPACITOR POL | SENSOR | PRECOND.SCH |
| C12 | 470pF | CAP | SENSOR | PRECOND.SCH |
| C14 | 22uF | CAPACITOR POL | SENSOR | PRECOND.SCH |
| C16 | 20pF | CAP | SENSOR | PRECOND.SCH |
| C17 | 20pF | CAP | SENSOR | PRECOND.SCH |
| C2 | 22uF | CAPACITOR POL | SENSOR | PRECOND.SCH |
| C20 | | | | |
| C23 | | | | |

SENSOR.EXP

| | A | B | C | D | E |
|---|---|---|---|---|---|
| 23 | Reference | Part Value | PCB Footprint | Rating | Tolerance |
| 24 | C16 | 20pF | CK05 | | |
| 25 | C17 | 20pF | CK05 | | |
| 26 | C20 | 470uF | CL25C2 | 25V | |
| 27 | R18 | 1K | RC07 | | |
| 28 | R15 | 10K | RC05 | 1/4W | |
| 29 | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
| 30 | R1 | 470K | RC05 | 1/4W | |
| 31 | C1 | [illegible] | [illegible] | [illegible] | [illegible] |
| 32 | [illegible] | [illegible] | [illegible] | [illegible] | [illegible] |
| 33 | C12 | 470pF | CK06 | | |
| 34 | R21 | 470 | RC05 | 1/4W | |

Microsoft Word - NOISE.DOC

We have identified the reason for the recent incidence of excessive noise in the prototype runs. Our recommendation to pursue a new manufacturer for the 22uF caps is based on our findings after sampling lots of seven different date-codes. The parts in question have demonstrated unacceptable noise performance.¶

¶

Fig. 1 Input stage from PRECOND.SCH¶

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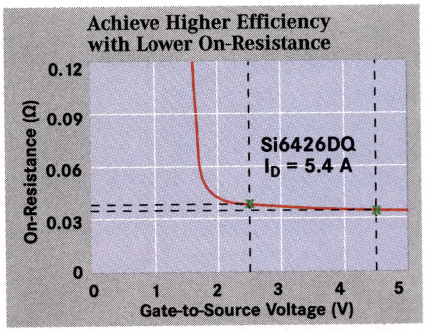

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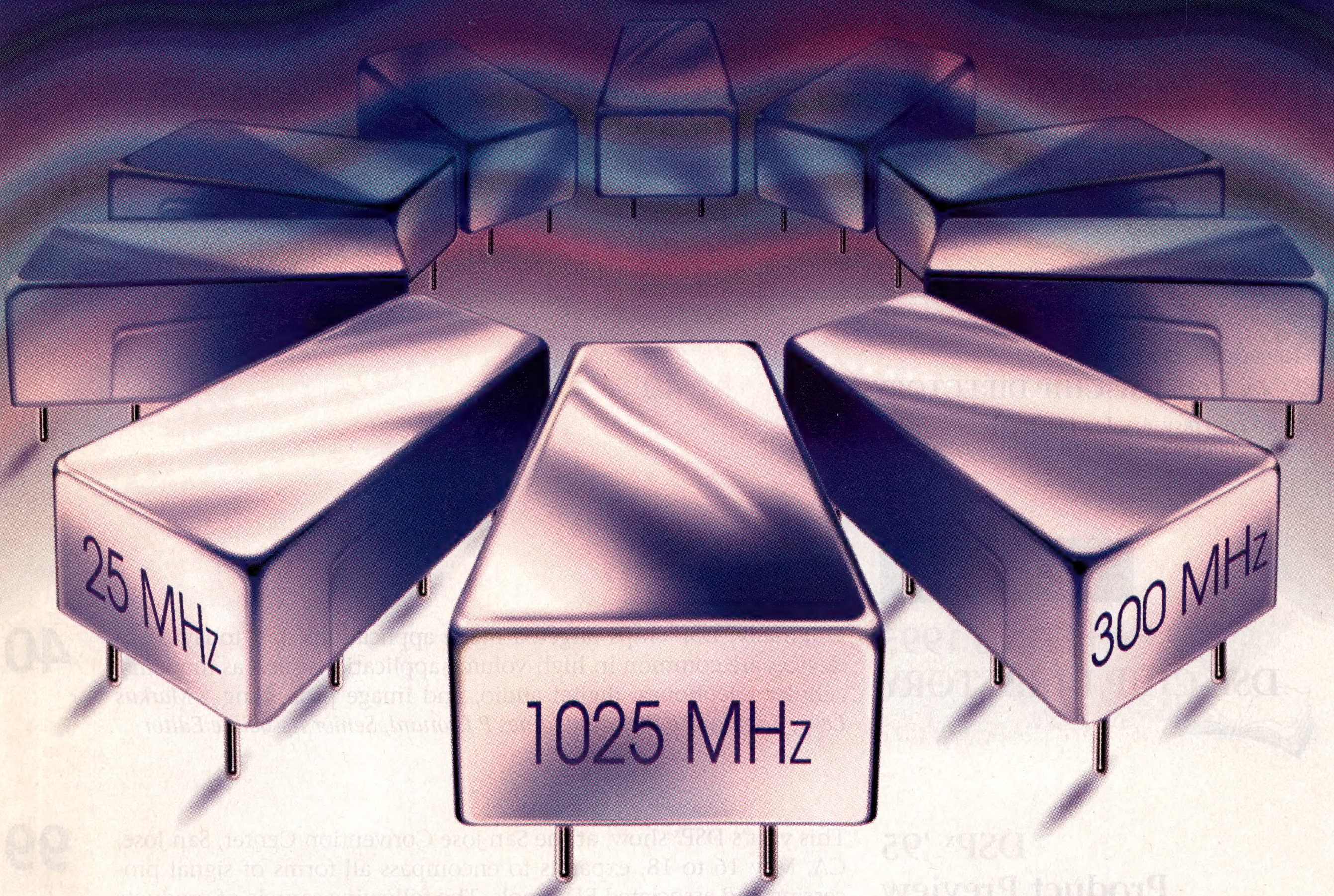

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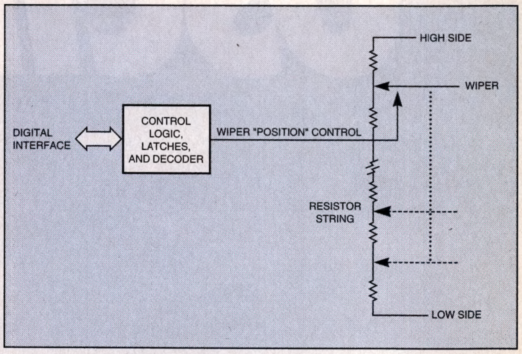


**Gain control goes silicon** 113

## COVER STORY

**EDN's 1995 DSP-CHIP DIRECTORY** 40

*(Photo courtesy Analog Devices)*

## EDN

## DESIGN FEATURES

**EDN's 1995 DSP-CHIP DIRECTORY**
Originally, DSP chips targeted niche applications, but today these devices are common in high-volume applications such as modems, cellular telephones, digital audio, and image processing.—*Markus Levy, Technical Editor, and James P Leonard, Senior Associate Editor* 40

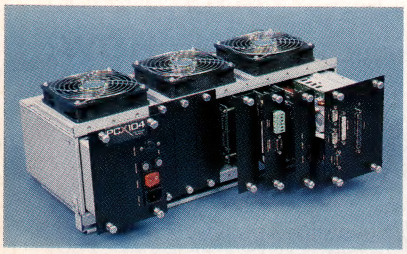
**DSPx '95 Product Preview**
This year's DSPx show, at the San Jose Convention Center, San Jose, CA, May 16 to 18, expands to encompass all forms of signal processing and associated EDA tools. The following sample of products gives you a glimpse of the tremendous variety of the DSPx exhibits. —*Steven H Leibson, Editor in Chief* 99

**Gain control goes silicon**
Increasingly, ICs are replacing mechanical potentiometers for gain control, providing both flexibility and compactness. However, you must choose carefully from among available architectures. Incompatibilities, limitations, and unique architectures complicate the final choice.—*Bill Schweber, Technical Editor* 113

**Detailed model shows FPGAs' true costs**
Design decisions are far more complex than simply weighing the unit price and NRE charge to determine whether to use FPGAs or ASICs. An analysis of all the variables affecting IC development shows that FPGAs are extremely cost-effective at surprisingly high production volumes.—*Joseph Liu, Xilinx Asia Pacific* 153

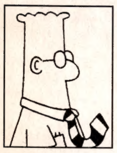
**Simulation backplanes allow concurrent use of multiple simulators**
Like hardware-backplane standards PCI and SCSI, the standard calls in simulation backplanes allow you to connect multiple simulators for substantial gains in design productivity.—*Kevin Jorgensen and Peter Odryna, Precedence Inc* 165

## OUT IN FRONT



PCX104 bus ruggedizes PC104 **15**

16-bit device provides 80C51 upgrade path **15**



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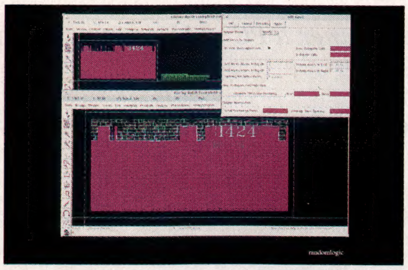
Programmable regulators are stable with any load **16**



Data-path compiler cuts design time in half **18**

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AT&T extends DSP16xx family with low-power version **22**

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Algorithm converts random variables to normal **130**

Two cores marry, make swinging choke **132**

Spice model simulates broadband transformer **134**

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Sync separator includes AGC **140**

Single IC adds analog inputs to digital PLC **144**

Synchronized window comparator eliminates error **146**

Token passing fits large counters into CPLDs **146**

## EDN COLUMNIST

Fuzzy-logic: an enabling technology **215**

As powerful as rule-based representation is, the use of fuzzy logic strengthens it in a number of ways.—*David Brubaker, Fuzzy-Logic Contributing Editor*

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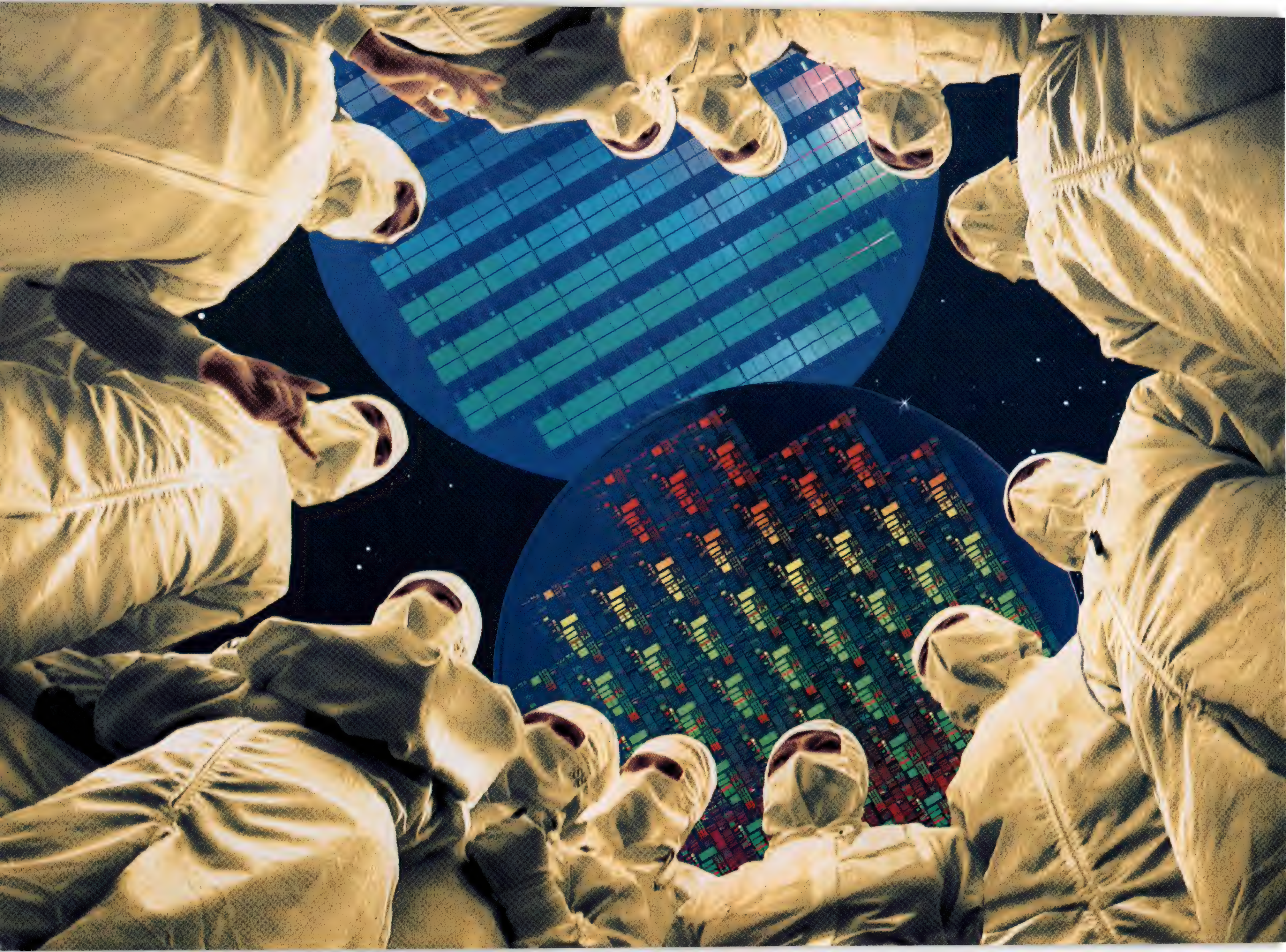
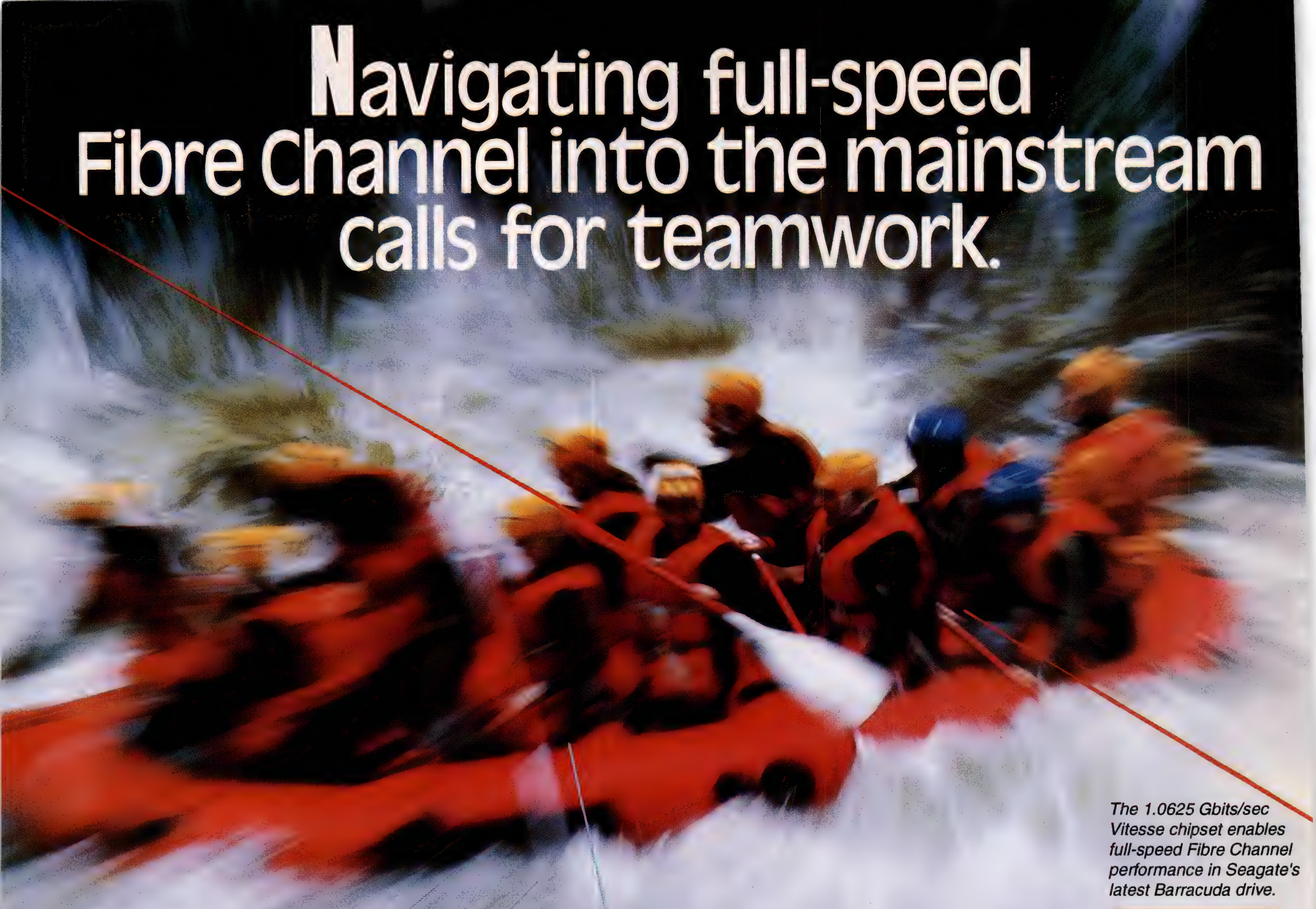
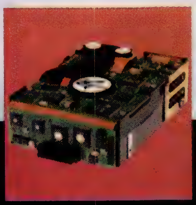




The 1.0625 Gbits/sec Vitesse chipset enables full-speed Fibre Channel performance in Seagate's latest Barracuda drive.



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# Time to volume

Recently, at Design SuperCon '95, co-sponsored by Hewlett-Packard and *EDN*, I attended a dinner held by HP. HP Chairman, President, and CEO Lew Platt gave an interesting speech. His two major themes were reducing "time to insight" and reducing "time to volume." I wrote about the first concept in the last issue of *EDN*. In this issue, I address "time to volume."

At one time, the only high-volume electronic products were consumer products, such as radios and TVs. That's changed. Last year, PCs outsold color TVs in the United States. Computer and communications products have now entered the high-volume arena, as have a number of companies, including HP, that have little previous experience with high-volume production—possibly yours.

**To cut the rejection rate to the ideal of zero, product design must accommodate a wide range of component margins.**

In 1987, HP's Vancouver Division built products at the rate of two to 3000 per month. Now, the division is responsible for building the company's DeskJet line of ink-jet printers. When it first started building these units, it produced them at 20,000 per month, roughly a tenfold increase in production-unit volume over the 1987 rate. The division expects soon to reach 1 million per month.

The demands on product design change substantially at such high production volumes. The first demand is an increased need for design margin. To cut the rejection rate to the ideal of zero, the product design must accommodate a wide range of component margins. At extremely high manufacturing volumes, you must achieve extremely low rejection and rework rates. Further, HP manufactures these printers at several sites worldwide. Perhaps your company is similarly arrayed around the world. Wide design margins help here, too.

However, margins aren't the only consideration for high-volume design. The pressures of high-volume manufacturing have forced HP to curtail the practice of designing a product and tossing it over the wall to manufacturing. The company now brings people from the lab, from manufacturing, from marketing, and from customer support together on the project team at the early, formative stages of a project. The different points of view contribute to better product design. Some HP divisions seat manufacturing engineers with design engineers to further collaboration.

Finally, HP finds that any means of improving communications among project-team members improves the product design, manufacturability, and, consequently, time to volume. Examples of communications technology involved include electronic mail and video conferencing. Now, with engineers on the same project scattered around the globe and in different companies, these electronic communications are becoming even more important.

Steven H. Leibson

**STEVE H LEIBSON**
**EDITOR IN CHIEF**

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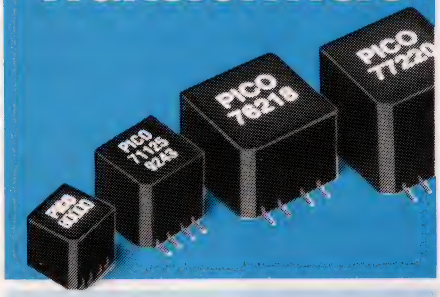

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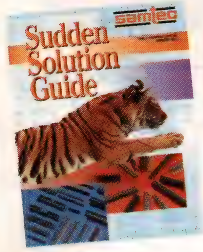

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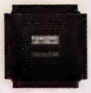

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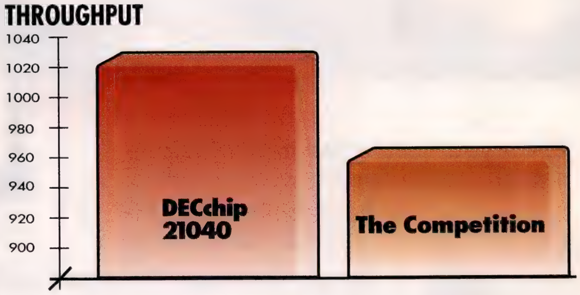

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# EDN OUT IN FRONT

*EDITED BY FRAN GRANVILLE*

## PCX104 bus ruggedizes PC104

Diversified Technology's PCX104, a ruggedized version of the IEEE-standard PC104 bus, addresses several PC104 shortcomings, including cooling problems and long mean time to repair. The main causes of PC104's drawbacks are its stacked-board architecture, its less-than-rugged connectors, and the physical problems of incorporating disk drives and other peripherals into a PC104 system.

Rather than using a stacked-board architecture, the PCX104 modules plug into a passive backplane through 96-pin DIN connectors. The modules slide into a card cage and employ metal front panels with captive fastening hardware for mechanical security. The cage and metal front panels add mechanical integrity and provide a mechanical foundation for as many as three cooling fans.

**Diversified Technology's PCX104 modules slide into a card cage and employ metal front panels with captive fastening hardware for mechanical security.**

The PCX104 standard retains the PC104's signal definitions and conforms to the IEEE PC96 bus-pinout specification. However, the PCX104 does not retain the PC104's mechanical characteristics or conform to the PC96 physical or electrical characteristics. However, you can incorporate PC104 cards into a PCX104 system by plugging the PC104 card onto an adapter module that plugs into the PCX104 backplane.

The company has developed a PCX104 backplane and card cage, a power-supply module, an i486DX/4-100 CPU module, an I/O module containing the standard PC I/O devices and ports, and the PC104 adapter module. A system comprising the card cage, power supply, backplane, CPU card, and I/O module costs $2695.

—by Steven H Leibson

**Diversified Technology**, Ridgeland, MS. (601) 856-4121. **Circle No. 435**

## Digital designer wanted

**If you're an accomplished digital-design engineer, *EDN* would like to hear from you. We're looking for a technical editor with the background and experience to interpret technical trends in digital design, computers, and peripherals for our 160,000 readers. As an editor, your primary responsibility will be to research, write, and edit articles. You'll also attend trade shows and meet with industry leaders. We need someone who likes people, communicates well, and can balance several projects with fixed deadlines. Writing experience is desirable, but not essential. We're looking for someone who lives in the Boston area or Silicon Valley. Our salaries are competitive with engineering positions. Please fax your resume and writing samples (if any) to Gary Legg, Executive Editor, at (617) 558-4470, or send via Internet to gary.legg@edn.cahners.com. *EDN* is an equal-opportunity employer, M/F/D/V.**

## 16-bit device provides 80C51 upgrade path

Philips' new XA-G3 microcontroller is the first to incorporate the 16-bit XA architecture. The architecture, which the company announced in September, provides an upgrade path for the 8-bit 80C51. The company sees the upgrade path as important because an increasing number of applications require 16-bit performance, although 80C51s continue to thrive.

According to market-research company In-Stat, Scottsdale, AZ, the market for 8-bit µCs will grow 40% by 1998, with worldwide sales increasing from $5 billion now to $8 billion in 1998. Meanwhile, worldwide sales of 16-bit µCs will grow more than 60%—from $0.9 billion to almost $3 billion in 1998. (Motorola recently shipped its 1 billionth 68HCO5, and vendors have shipped more than 1.5 billion 80C51-based µCs.)

The XA architecture supports the 80C51's memory map, registers, and instructions. Although you must reassemble 80C51 source code to run on the XA, translation is one-to-one and does not require multi-instruction constructs.

The XA architecture features 16-bit registers, an

*(continued on pg 16)*

internal data path, and a CPU. You can configure the external bus as 8 or 16 bits, and you can use some of the upper address lines as I/O ports, depending on the amount of memory the application requires. The devices support multitasking via banked-switched registers, and you must write a supervisory program that determines when and for how long each task runs.

The architecture has up to 32 vectored interrupts and exception-handling circuitry for fault-tolerant systems. Software controls standby and power-down modes: Standby leaves most of the on-chip peripherals and external interrupts functioning; power-down shuts down everything, including the on-chip oscillator.

The XA-G3 features 32 kbytes of EPROM/ROM, three counter/timers, a watchdog timer, two UARTs, and a 12- to 20-bit address bus for up to 1 Mbyte each of program and data. The static-core G3 operates from 2.7 to 5V. It is available in 40-pin DIP and 44-pin PLCC/TQFP packages and costs $7 (10,000).

—by Markus Levy

**Philips Semiconductors**, Sunnyvale, CA. (800) 234-7381.

**Circle No. 436**

**NASA seeks licensees for invention.** The National Aeronautics and Space Administration (NASA) is seeking licensees to produce low-cost, high-performance components and systems based on an electronic measurement circuit delivering better accuracy than previous methods. The invention, the Anderson Current Loop, prevents errors caused by variations in the wires that connect sensors to data-collection equipment. Karl Anderson, a senior measurement systems engineer at NASA, developed the circuit. Contact the Office of Chief Counsel, NASA Dryden Flight Research Center, Box 273, Edwards, CA 93523-0273.

**NASA**, Edwards, CA. (805) 258-3449.

**Circle No. 437**

## PROGRAMMABLE REGULATORS ARE STABLE WITH ANY LOAD

Linfinity's new LX6431 family of progammable shunt regulators has unconditional dynamic stability for all practical values of capacitive output loading, according to the company. Thanks to this stability, designers can choose the value of output capacitor that yields the optimum transient response without fear of oscillation.

In contrast with industry-standard 431 regulators, which have two internal poles that conspire with capacitive loading to produce instability, the LX6431 has only one internal pole. It also uses a pole-splitting technique to separate (in frequency) the internal pole from the external pole created by capacitive loading.

The LX6431 devices also require much less input-reference current (0.5 μA max) than other 431 regulators. You can thus use higher value divider resistors to program the output voltage. The lower input current also reduces the voltage error arising from current flow through the divider network.

Using two external resistors, you program the output voltage to a value of 2.5 to 36V. The regulators spec a 100-mΩ max output impedance at output currents ranging from 0.6 to 100 mA. The plastic-packaged LX6431 is available in eight-pin SOICs and three-pin TO-92 and SOT-89. $0.53 to $1.25 (1000).—by Bill Travis

**Linfinity Microelectronics Inc**, Garden Grove, CA, (714) 898-8121 **Circle No. 438**

**SGS-Thomson opens design center in India.** SGS-Thomson Microelectronics has opened a design center in Noida, India. The 5000m² building will house the company's largest design facility outside Europe.

**SGS-Thomson Microelectronics Inc**, Lincoln, MA. (617) 259-0300. **Circle No. 439**

**DILBERT® by Scott Adams**

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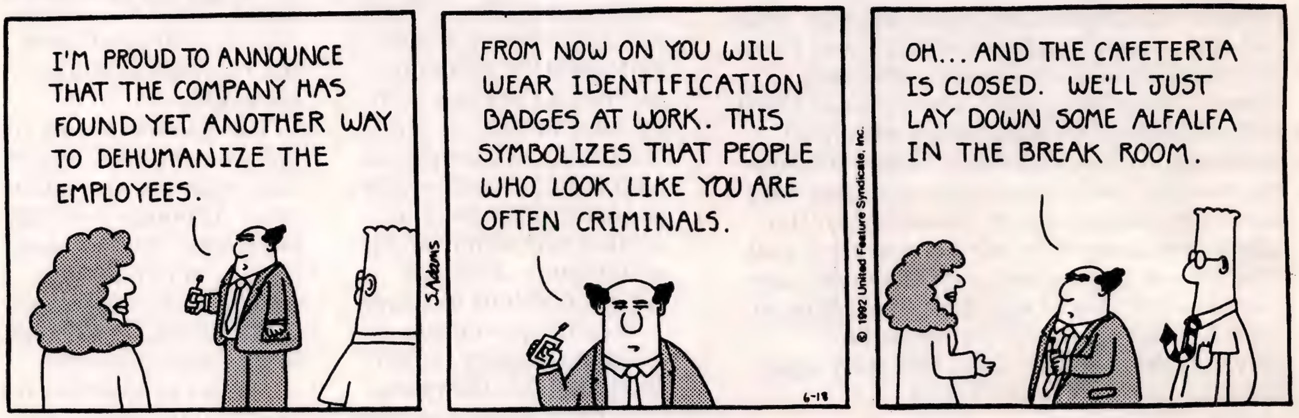
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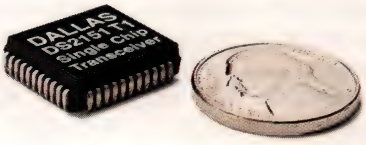

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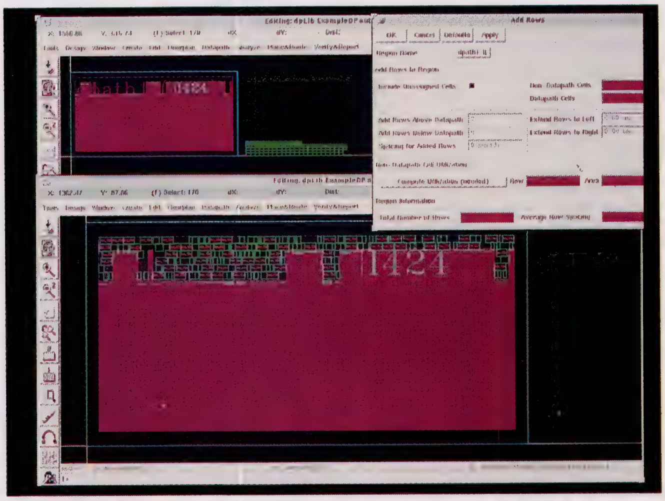
# Data-path compiler cuts design time in half

Cadence Design Systems' new Smartpath data-path compiler for ASIC-chip design, cuts data-path design time in half and produces results that rival custom-designed data paths in performance and area, according to the company. DSP, µP, and µC chips make heavy use of data paths, so improvements in data-path design time and efficiency can provide direct time-to-market and performance benefits to systems that use these chips.



**By embedding random logic (green) within the data-path block (magenta), Smartpath minimizes data-path size and interconnection distance between the data path and control logic.**

Smartpath's design methodology is based on the ability to embed random or control logic within the data-path block, the interleaving of data-path functions, and over-the-cell routing for bit-swapped buses. Embedding control logic within the data-path block decreases interconnection distance between control and data-path functions, resulting in higher performance and smaller dice. Interleaving data-path functions eliminates channels between cell rows, letting you experiment with data-path block aspect ratios to fit the block within empty regions on the chip. By routing over cells for bit-swapped buses, Smartpath conserves data-path area. Some other data-path-generation schemes require additional routing channels and extra chip area to accommodate bit swapping between data-path buses.

Smartpath employs your own or Cadence's 0.5-µm standard cell library, and you can supplement the library with user-configurable cell generators, such as adders, multipliers, and shifters. You can change cell-generator parameters, such as word width or drive capability by specifying parameter values on a screen menu and then have Smartpath automatically compile the desired block.

You input information to Smartpath from Cadence's Composer schematic editor or from the Verilog hardware-description language. Cadence will support VHDL input in a future release.

Smartpath is available as an option to the Preview floor planner and the Cell3 Ensemble or Cell Ensemble place-and-route software packages. Prices start at $40,000. An optional data-path compiler for Verilog costs $15,000. Cadence's standard-cell library adds $200,000 to the cost.—by Jim Lipman

**Cadence Design Systems**, San Jose, CA. (405) 943-1234. **Circle No. 440**

## A/D CONVERTER OFFERS FEATURES FOR SOFTWARE RADIOS

Analog Devices' new low-distortion, high-speed AD9042 converter suits use in "software radios," which use a single wideband receiver operating over the entire 12.5-MHz-wide cellular band. The device allows cellular base stations to support multiple standards using software-defined hardware, rather than an array of dedicated receiver channels that may have the wrong mix at any instant. The device supports the Advanced Mobile Phone Service (AMPS), narrowband AMPS, time-division multiple-access, and Cellular Digital Packet Data standards, among others. It features 12-bit resolution, a 41M-sample/sec minimum sampling rate, and a 50M-sample/sec typical sampling rate (twice that of comparable A/D converters). Software decodes the digitized aggregate signal (representing up to 60 user channels), leaving the base station available to handle an arbitrary mix of standards and changing the mix dynamically as user demands change.

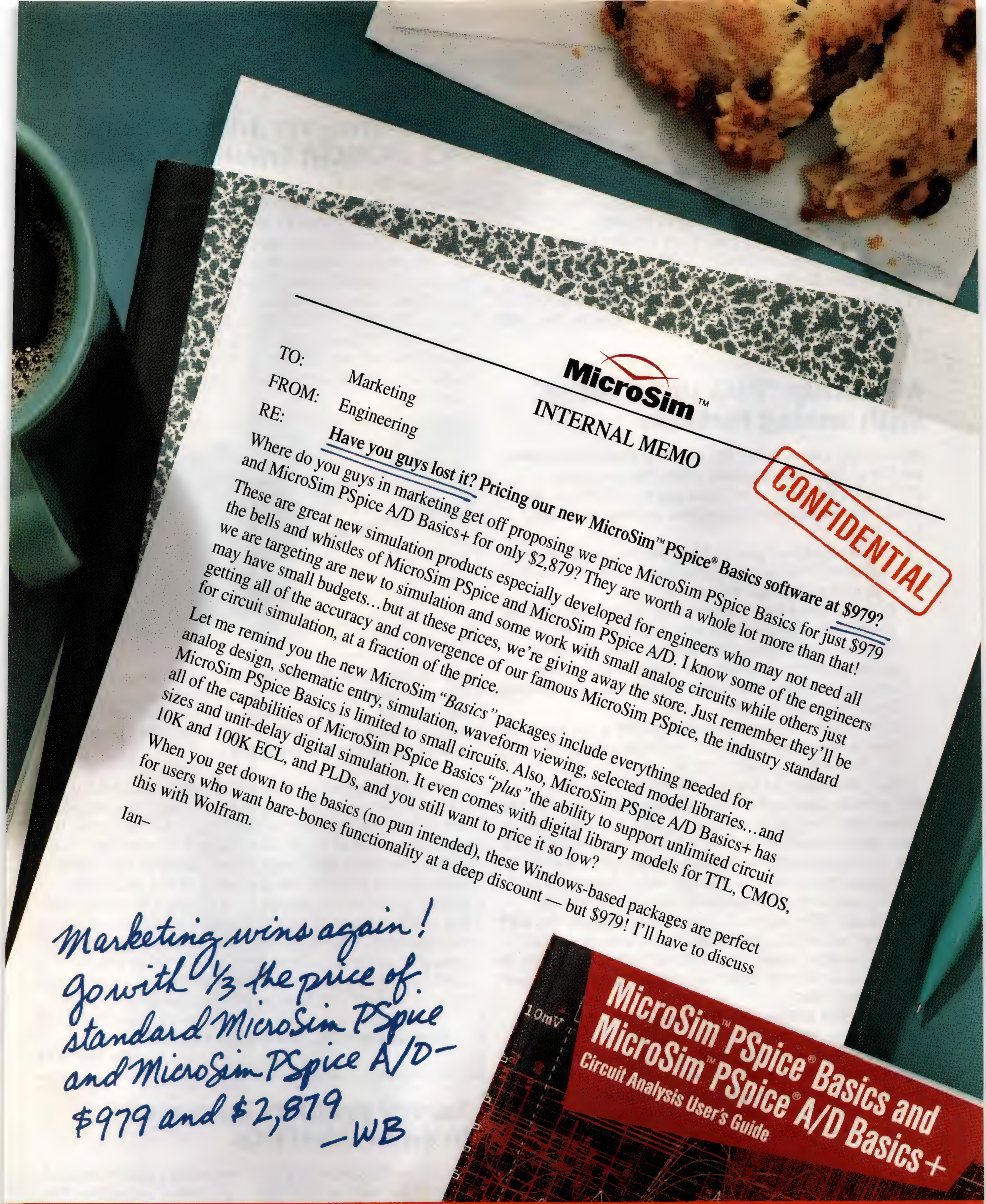
The company tests the monolithic device with up to 48 input tones, compared to the two or three tones in a conventional test, to more closely simulate actual use. Spurious-free dynamic range is more than 80 dB with a 20-MHz input signal (Nyquist frequency), and power consumption is 575 mW with a 5V supply. The AD9042 is available now in a ceramic DIP for $199 (1000) and will be available in October in a surface-mount plastic package for $49.—by Bill Schweber

**Analog Devices Inc**, Norwood, MA. (617) 937-1428. **Circle No. 441**

## Chip bridges PCI to 68040

The Spanner interface chip from Newbridge Microsystems is the first in a family of Peripheral Component Interconnect (PCI)-to-68040 bridge chips that the company is developing with Motorola. The Spanner allows designers of high-performance embedded systems to retain their existing 68000 code, lower the cost of their products, and decrease their time to market, according to the companies. The chip suits applications, such as 68360 communications

*(continued on pg 20)*



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CIRCLE NO. 190

controllers, in which the 68000 design functions as a CPU in the PCI system.

The Spanner chip offers a 32-bit PCI interface, can be adapted to other 680x0 buses, and is optimized for high throughput between a 68040 initiator and a PCI target. The device supports Joint Test Action Group testing and offers two programmable slave images on the PCI interface. The Spanner comes in a 225-pin ball-grid-array package and costs $39 (10,000).

—by Fran Granville

**Newbridge Microsystems**, Kanata, ON, Canada. (613) 592-0714.

**Circle No. 442**

## Microchip "PICs up" 8-bit µC with analog features

Microchip's new 8-bit PIC16C622 microcontroller, which is code-compatible with the company's PIC16CXX µC line, performs up to 5 MIPS at 20 MHz. The device also supports analog features, including

- TTL brown-out protection with a programmable detection period that resets the CPU when the voltage drops below 4V
- Dual voltage comparators (±10 mV) with eight programmable modes and the option to interrupt or wake up on transition. You can program coefficients for the comparators into one-time-programmable (OTP) memory during final test calibration.
- A voltage-reference module with a 16-tap resistor ladder that supports voltage ranges from $V_{SS}$ to 75% $V_{DD}$ and 25% $V_{DD}$ to 75% $V_{DD}$.

Like the register-based PIC16CXX µCs, the PIC16C622 employs a Harvard architecture for separate code and data and has a 14-bit-wide instruction set. Unlike the PIC16CXX µCs, the PIC16C622 has a watchdog timer with a dedicated on-chip RC oscillator for system wake-up. Additionally, the device contains 128 bytes of data RAM and a 2k×14-bit OTP memory. You can program the OTP memory using the PIC16C622's in-circuit serial programming mode. The PIC16C622 is available in 18-lead plastic DIP/SOIC or 20-pin SSOP packages for $2.98 (1000).

Microchip offers several development tools to support the PIC16C622. The $3750 PICMASTER-16H universal development system includes an emulator-control pod, a target-specific emulator probe, and a prototyping programmer. The PICSTART-16C ($195) offers a development-software suite that includes an assembler, a simulator, and a simple programmer. To further help you with your development efforts, Microchip is conducting nationwide seminars from May to July.

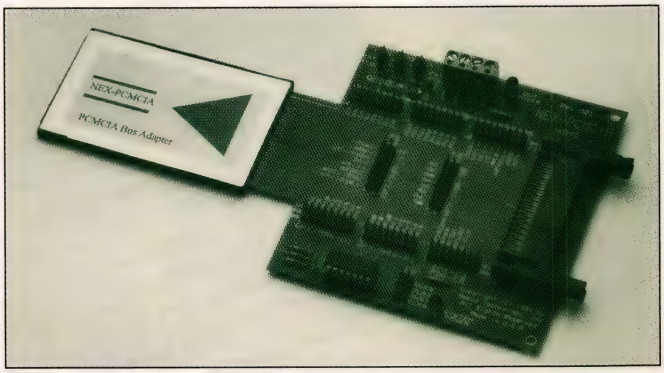
—by Markus Levy

**Microchip Technology**, Chandler, AZ. (602) 786-7200.

**Circle No. 443**

## Logic-analyzer adapters ease PCI, PCMCIA troubleshooting

A family of adapters from New Wave PDG greatly simplifies using Tektronix DAS 9200, Prism, and TLA series logic analyzers to troubleshoot popular buses. Besides making connections easier, the adapters make interpretation of the data more straightforward by tailoring the analyzers' displays to the bus. New Wave offers models—each costing $1595—for the Peripheral Component Interconnect (PCI), PCMCIA, VME, EISA, ISA, and MicroChannel buses. All of the adapters work with analyzers that that use 92A96, 92C96, 32GPD, and 32GPX acquisition cards. Some also work with 92A90 and 30MPX acquisition cards.



**Bus adapters from New Wave PDG tailor Tektronix logic analyzers to troubleshooting of six popular buses, including PCI and PCMCIA. Of the six adapter types, only this PCMCIA adapter also acts as a card extender. The others plug into an unused slot on the bus under test.**

With the exception of the PCMCIA adapter, which also acts as a card extender, the adapters plug into an unused slot of the bus you are monitoring. New Wave took this approach to avoid errors introduced by extenders' added lead inductance and capacitance. Among the adapters convenience features are: grouping of the logic-analyzer podlet connections, grouping of logical channels, labeling of timing signals on the display, symbolic triggering (for example, trigger on I/O RD8 at a specific address), state and symbolic disassembly displays that use custom clocking to acquire addresses and data at appropriate times, and symbolic translation of acquired bus cycles.

—by Dan Strassberg

**New Wave PDG**, Norwood, MA. (603) 595-8116.

**Circle No. 444**

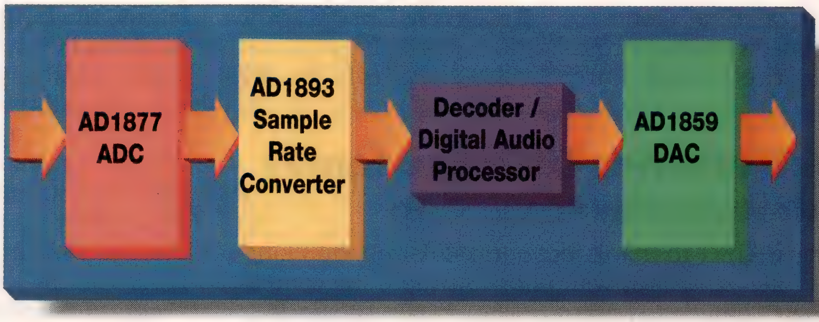
## Survey predicts increase in embedded PCs

The PC architecture is moving quickly into embedded systems, according to a recent survey of embedded-system developers. Within two years, predicts technology-research company Embedded Systems Research, embedded PCs will control

(continued on pg 21)

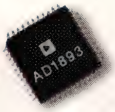
# CD-Quality Audio Converters At Prices That Sound Even Better.

When leading OEMs design tomorrow's audio products, they naturally talk to Analog Devices about high-performance digital audio ICs with true CD quality. For example, the ADC, sample-rate converter and DAC listed below all offer better than 90 dB dynamic range, dual channels and many unique multimedia audio features – all at low consumer OEM prices.

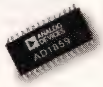


**AD1877 ADC.** This single-supply 16-bit sigma-delta stereo ADC provides 92 dB signal-to-noise ratio and -90 dB THD+N. Analog inputs are single-ended for easier use. A flexible serial data interface has eight user-selectable modes. There's even a 10 µW power down mode. Other applications include general-purpose data acquisition, communication systems and medical electronics. A -55° C to 105° C temperature-screened version is also available. Priced from $10.00.*

SAMPLEPORT

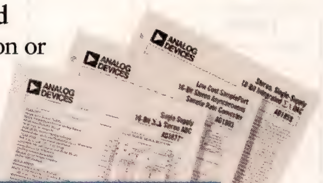


**AD1893 ASRC.** This SamplePort® stereo asynchronous sample rate converter has 96 dB dynamic range and -96 dB THD+N at 1 kHz. Our patented technology allows conversion over 1:2 or 2:1 sample frequency range and rejects sample clock jitter. Low power 3 V operation is perfect for portable applications like MiniDisc, CD-R and DAT. Prices start at $10.10.*



**AD1859 DAC.** This single-supply 18-bit integrated stereo DAC has 96 dB dynamic range, and -90 dB THD+N. A unique digital phase-lock loop accepts a 27 MHz master clock input and sample rates from 28 to 52 kHz, without external components. It's ideal for digital cable and DBS settop decoders, HDTV, CD players and high-end computer multimedia. Prices start at $7.00* for both SOIC and SSOP versions.

**Find Out How Silicon Should Sound.** For technical information or data sheets contact your local Analog Devices sales office or representative listed below.



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* USD 1,000s, recommended resale, FOB U.S.A.

SamplePort® is a registered trademark of Analog Devices, Inc.

CIRCLE NO. 12

34% of all embedded systems, up from 20% today. The PC architecture's rapid rise will come at the expense of custom controllers, which will decrease from 39 to 28%.

Out-sourcing of development and manufacturing is also a trend in embedded systems, according to the survey. Only 50% of survey respondents expect to design and build their own systems within two years, compared with 63% today. These and other survey results appear in a 134-pg report that sells for $495.—by Gary Legg

**Embedded Systems Research**, Corvallis, OR. (503) 754-9310.

**Circle No. 445**

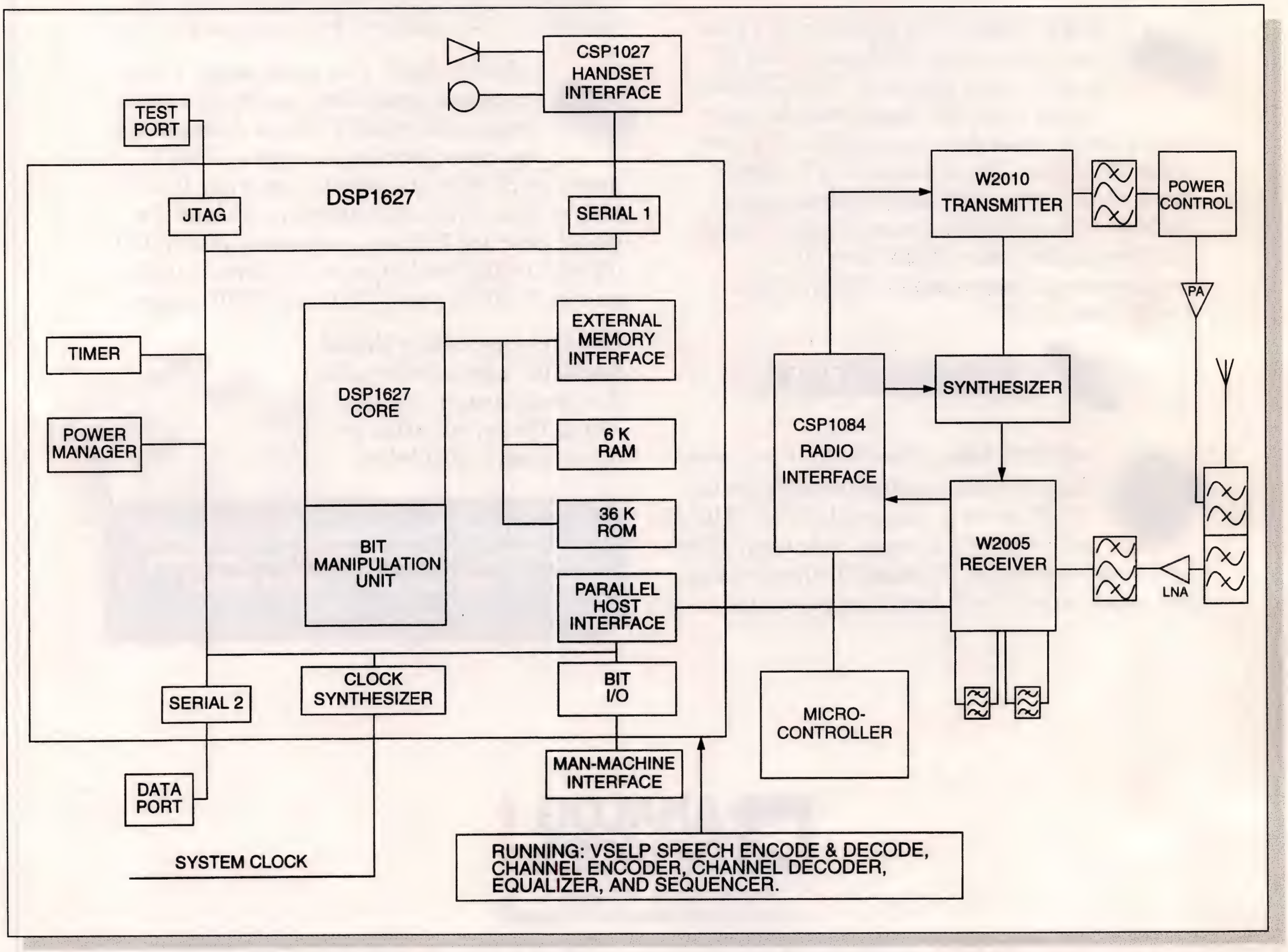
## AT&T extends DSP16xx family with low-power version

You have AT&T to thank for your cellular phone's long battery life—that is, if your phone includes the company's new 16-bit, fixed-point DSP1627 DSP. The device, based on the DSP1600 core and built on 0.5-µm technology, operates at 2.7V and typically consumes only 39 mA (98 mA typ at 5V), approximately five times lower than its predecessor, the DSP1617. The DSP has several power-management modes that let you selectively power down on-chip peripherals. However, the device's data sheet lacks a maximum-current-consumption spec, making it difficult for you to spec a worst-case battery life for your product.

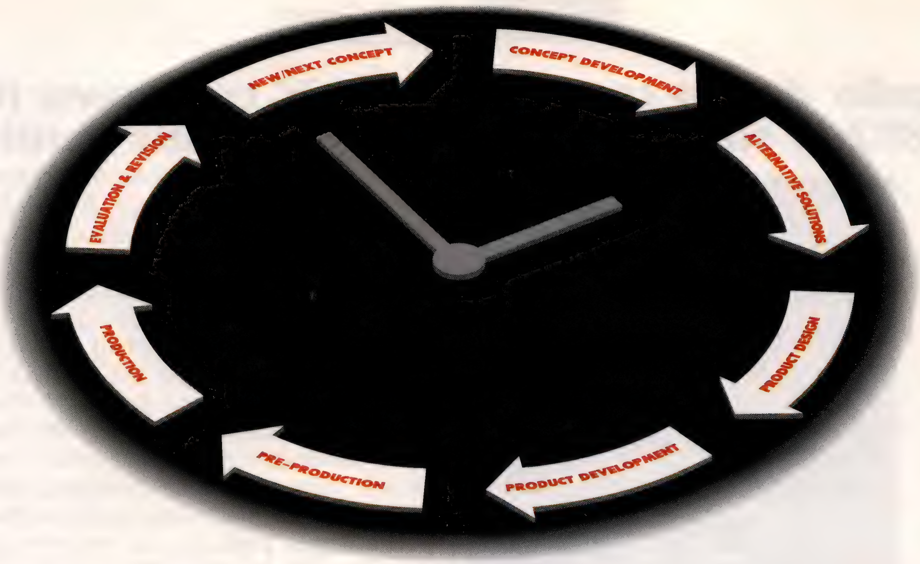
In addition to the standard features of the DSP16xx family, the DSP1627 integrates a bit-manipulation unit (BMU), a PLL, and an 8-bit parallel host interface. For speech coding, the BMU lets you perform barrel-shifting, normalization, and bit-field extraction/insertion operations. You can use the PLL rather than an external crystal to generate the system clock, helping to reduce EMI. You can use the parallel host interface for a no-glue attachment to either Intel or Motorola microcontrollers. The DSP1627 in a 100-pin PQFP/TQFP costs $45 (10,000).—by Markus Levy

**AT&T Microelectronics**, Allentown, PA. (800) 372-2447.

**Circle No. 446**



**AT&T's DSP1627 provides a minimal-chip-count and minimal-glue-logic implementation of a digital cellular phone. It integrates a bit-manipulation unit, a PLL, and an 8-bit parallel host interface. For speech coding, the BMU lets you perform barrel-shifting, normalization, and bit-field extraction/insertion operations.**



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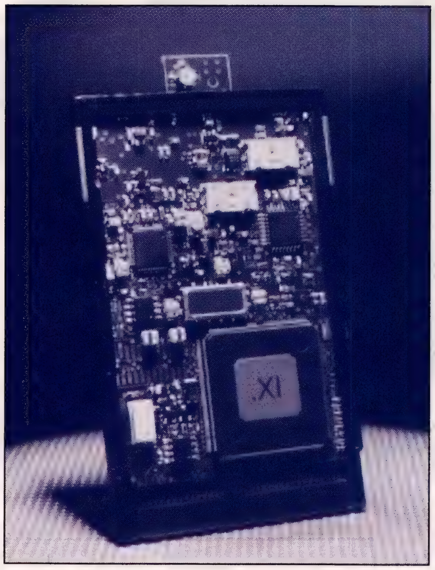
## 2.4-GHz radio design complies with IEEE 802.11 standard



The 2.4-GHz radio design on a PCMCIA card complies with IEEE 802.11 standard.

A new, high-performance radio design from Symbionics suits use in 2.4-GHz wireless LANs. The company based the design on the emerging IEEE 802.11 industry standard. By using common silicon instead of expensive GaAs to build a wireless LAN adapter, the design benefits manufacturers by allowing rapid production of inexpensive, standards-based, wireless-LAN products.

The small, low-power radio uses surface-mount technology. The design does not incorporate punched holes in the board; instead, components are soldered to conductive pads on both sides of the board's surface.

The radio achieves a –85-dBm sensitivity and a 20-dBm, or 0.1W, transmission power. The IEEE 802.11 standard mandates greater than –85-dBm sensitivity and 30-dBm, or 1W, of maximum allowed power. The radio suits frequency-hopping transmission. Manufacturers that want to incorporate wireless capability into their products can license the design, reducing time to market and development costs, according to the company. The license costs $40 or less.—by John Gallant

**Symbionics Networks Ltd**, Cambridge, UK (+44) 122 342 1025. **Circle No. 447**

## RS-232C transceiver IC has 1μA automatic shutdown

As an additional strategy for minimizing power consumption, the shutdown mode in the MAX3218 dual-channel transceiver from Maxim is self-contained, working without any software directive. The IC monitors its receiver inputs, and, if there is no valid RS-232C level (mark or space) on those inputs, the IC automatically puts itself into shutdown mode, reducing supply current to 1 μA. (Absence of valid levels indicates either that the interface cable is disconnected or that the peripheral device is turned off.) When either input senses a valid level, the IC turns itself back on. Because the IC defines the shutdown function, you can use the IC to replace drivers without changing system software. The device also provides a hardware shutdown-control line.

The device provides two receiver and two transmitter channels and operates with a supply range of 1.8 to 4.25V, and supports a 120-kbps data rate. It comes in 20-pin SSOP and DIP packages and costs $1.92 (1000).

—by Bill Schweber

**Maxim Integrated Products**, Sunnyvale, CA. (408) 737-7600, ext 6087. **Circle No. 448**

**Video chronicles semiconductor industry.** The "Silicon Genesis Project" will chronicle the history of the semiconductor industry on videotape. Semiconductor industry veteran and LSI Logic founder Rob Walker and others, in cooperation with Stanford University Libraries, plan to produce and fund the project. The tape will include a series of interviews with important figures in the semiconductor industry, including Dr C Lester Hogan, former general manager of Motorola Semiconductor and CEO of Fairchild Semiconductor; John Pierce, who coined the term "transistor" while at Bell Laboratories; and Marcian "Ted" Hoff, inventor of the μP. The videotapes will be available for researchers at the Department of Special Collections, Stanford University Libraries. Contact Dr Henry Lowood.

**Stanford University**, Stanford, CA. (415) 723-4602. **Circle No. 449**

## Resizing engines offer shrink and zoom operations

After a successful sampling program, Genesis Microchip's three new video/image DSP chips, the gm865x1 and gm833x2 resizing engines and the gm2242B half-band filter, have entered volume production. The resizing engines use the company's Acuity Resizing series of real-time 2-D filtering engines to perform shrink and zoom operations. Acuity Resizing devices produce high-quality scaled images and reduce aliasing, artifacts, and distortion that are common with digital video scaling. Both chips use interpolating and FIR filtering. When in reduction mode, the chips have all memory on chip for FIR filtering.

The gm865x1 ($59 (50,000)) offers up to 65-tap vertical and up to 65-tap horizontal filtering independently in both directions. The chip suits use in medical-imaging and LCD-projection systems and high-end broadcast equipment, which can take advantage of the chip's dynamic horizontal resizing for special effects.

The gm833x2 ($23 (50,000)), offers up to 33 taps and suits use in videographic workstations, multimedia systems, and projection and scan-conversion equipment.

The gm2242B half-band filter ($15.24 (50,000)) is compatible with the industry-standard TMC2242B chip and features a user-selectable sinx/x compensating filter, a pass-through mode, and constant data latency. Applications include broadcast and teleconferencing systems and digital-compression and encoder equipment.—by Fran Granville

**Genesis Microchip Inc**, Markham, ON, Canada, (905) 470-2742. **Circle No. 450**

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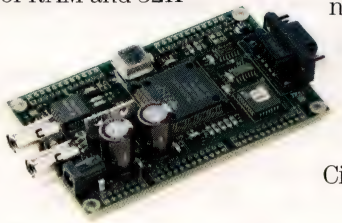

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* Suggested resale price, U.S. dollars.

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## Verification tool suite for submicron chips runs more efficiently

Integrated Silicon Systems (ISS) has released version 2.5 of the VeriCheck hierarchical verification system for submicron chips. The version uses a new connectivity data structure that substantially reduces the runtime and system memory for physical verification of complex ICs.

Back-end design of complex chips requires verification of the layout database to ensure design success. Performing this verification on multimillion-transistor circuits can take substantial time. ISS claims that VeriCheck 2.5 cuts layout-vs-schematic runtime in half and improves design-rule-checking runtime by 20%, allowing you to run full verifications on complex chips in a day.

The VeriCheck 2.5 package comprises four "traditional" verification tools. A hierarchical design-rule checker (HDRC) checks the layout database for correctness. A hierarchical layout-vs-schematic (HLVS) checker compares an extracted netlist from a layout database to a netlist derived either from a schematic or from another layout. A hierarchical electrical-rules checker (HERC) tests for such circuit violations as transistor gates shorted to power or ground, unconnected inputs or outputs, and nets with excessive fan-out. A hierarchical layout-parameter extractor (HLPE) extracts device-parameter information from a layout database for use in a Spice netlist. The suite also includes the RCE critical-net RC extractor, the VeriView graphical debugging tool, and the VeriAccess C-language procedural interface.

VeriCheck 2.5 tools run on Digital Equipment, Hewlett-Packard, IBM, and Sun platforms. Prices are $60,000 for HDRC, $70,000 for HLVS, $40,000 for HERC, $50,000 for HLPE and $30,000 for RCE. Prices for VeriView and VeriAccess start at $25,000 each. Using Cadence's standard-cell library adds about $200,000.—by Jim Lipman

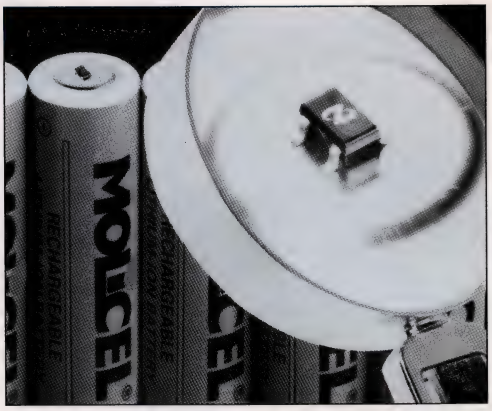
**Integrated Silicon Systems**, Research Triangle Park, NC. (919) 361-5814.

**Circle No. 452**

## Lithium-ion battery-charge controller suits various charging approaches

National's LM3420 IC for charge and end-of-charge control of lithium-ion batteries works in linear, switching, and isolated high-efficiency switching charging. Because lithium-ion batteries have approximately half the weight and 70% of the volume of NiCd batteries, the lithium-ion units are enjoying growing popularity for handheld and portable equipment. The charge controller is available for one-, two-, or three-cell operation (4.2, 8.4, and 12.6V, respectively) and in ±0.5 and ±1% tolerances, providing up to 15 mA of output current into external circuitry.

The device comes in a five-pin SOT23 package that has 20% of the footprint of an eight-pin SOIC. Despite its size, however, the IC includes a precision bandgap reference that is trimmed and curve-corrected for operation over the –40 to +85°C range, an internally compensated op amp, voltage-setting resistors, and an npn output driver. The LM3420 costs $1.05 for the ±0.5% grade and $0.90 for the ±1% grade (1000).—by Bill Schweber



**National's LM3420 controller IC, in an SOT23-5 package, supports charging of one-, two-, and three-cell lithium-ion batteries.**

**National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959.

**Circle No. 451**

### CALENDAR OF UPCOMING EVENTS . . .

**May 16 to 18, 1995**
DSP$^x$, San Jose, CA, is the signal-processing show for the design community. Co-sponsored by *EDN* and Reed Exhibition Co, Norwalk, CT. (203) 840-5652.

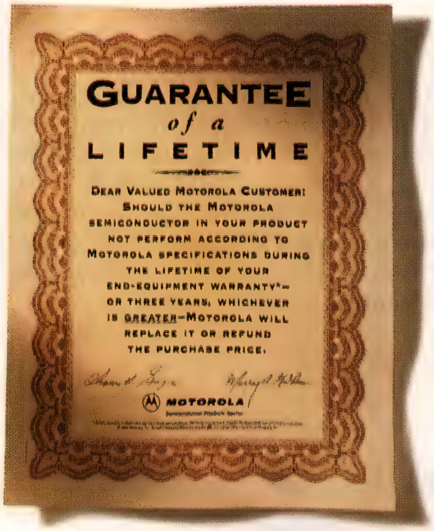
**June 12 to 16, 1995**
Intertronic '95, Paris, features sessions and exhibits on active and passive components, subcontracting, and production and test-and-measurement equipment for the European market. Blenheim Division Industries, Levallois Perret Cedex, France. (+33) 1 47 56 50 00.

**June 18 to 22, 1995**
IEEE International Conference on Communications, Seattle, offers tutorials on communications and networking topics, papers on current trends, and exhibits. IEEE, Seattle, WA. (206) 616-1596.

**June 21 to 23, 1995**
Electro '95, Boston. This three-day electronics event has tutorials, sessions, more than 600 exhibit booths, and a new-product showcase. Sponsored by the IEEE and the Electronics Representatives Association. (800) 223-7126.

**June 27 to 28, 1995**
VMIC Conference, Santa Clara, CA, covers conductor and dielectric systems and parasitic and noise evaluations. Dr Thomas Wade, University of South Florida, Tampa, FL. (813) 974-4779.

# The brain.



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### ANOTHER JFET SOURCE

We hope Javier Guadalajara's search for a 2N5565 is over ("Ask EDN," Oct 13, 1994, pg 22) and he is happy. If not, InterFET Corp of Garland, TX, manufactures semiconductor components, including endangered and extinct JFETs. But, considering the advances in materials and processes, Guadalajara may be better served with a more modern and efficient component. Considering the 2N5565 specifications, perhaps a Tetrode, a circular JFET, or an IC JFET would do. Contact Dan Roberts at InterFET ((214) 487-1287) for a data book.

*John Cail*
*Richardson, TX*

### ACCELEROMETER, ANYONE?

I'm in search of low-cost accelerometers for a consumer product I'm designing. The measurement range should be at least ±10g. Any suggestions on where to begin?

*Antonio Bersani, EE*
*Milan, Italy*

### QUIESCENT CURRENT TOO HIGH

I am working on a magnetic-detector-based project using the Philips KMZ10. Because the final application has to be portable, a battery will supply the current. I have solved the problem of detection using my Design Idea (#1564, "Simple RC eliminates voltage reference," *EDN*, Aug 4, 1994, pg 71), but I still need to solve another problem: The 4-mA quiescent current for the KMZ10 is too high. Does anyone know of another type of magnetic sensor that would consume 0.5 mA on a 5V source? (I have checked models from Allegro, Honeywell, and Siemens without success.)

*Christophe Basso*
*Grenoble, France*

## Free Internet resources for engineers and programmers

Cera Research is offering three free "Frequently Asked Questions (FAQ) Roadmap" reports. "FAQ Roadmap: Embedded Systems Internet" identifies the key Internet resources, such as file-transfer-protocol (FTP) sites, Worldwide Web (WWW) sites, and Internet mailing lists, for embedded-systems programmers and design engineers. The report also has an index of IC manufacturers. "FAQ Roadmap: Windows Development Internet" identifies the key Internet resources, such as FTP and WWW sites and Internet mailing lists, for Windows programmers. It also points out useful archives of free shareware and the Microsoft Developer Network Internet sites.

"FAQ Roadmap: Search the Internet" targets engineers and programmers new to the Internet. It explains how to find resources for searching, such as key FAQ reports, Usenet groups, and other resources. It also has an index of WWW search engines.

To obtain these reports via FTP, type "ftp.best.com/pub/cera" or "ftp.netcom.com/pub/ce/cera." To obtain them via WWW, type "http: www.cera.com," and, to otbain them via electronic mail, type "email info@cera.com." —by Fran Granville

**Cera Research**, Newark, CA. (510) 713-1620. **Circle No. 453**

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| UC5602 | 18 | 11 | N |
| UC5608 | 18 | 6 | Y |
| UC5609 | 18 | 6 | Y |
| UCC5610 | 18 | 3 | Y |
| UCC5611 | 18 | 3 | Y |
| UC5603 | 9 | 6 | Y |
| UC5604 | 9 | 9 | N |
| UC5605 | 9 | 5 | Y |
| UCC5606 | 9 | 1.8 | Y |
| UC5612 | 9 | 5 | Y |
| UC5613 | 9 | 4.5 | Y |
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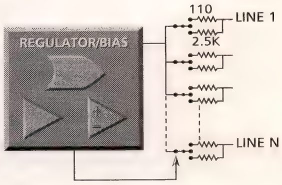

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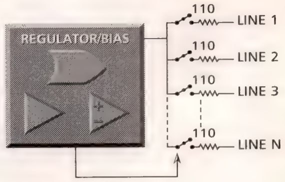

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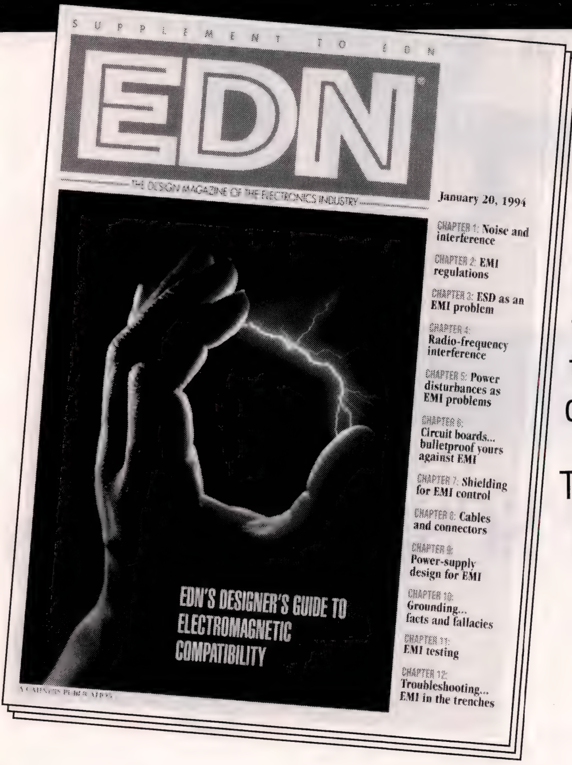

SUPPLEMENT TO EDN

EDN

THE DESIGN MAGAZINE OF THE ELECTRONICS INDUSTRY

January 20, 1994

CHAPTER 1: Noise and interference

CHAPTER 2: EMI regulations

CHAPTER 3: ESD as an EMI problem

CHAPTER 4: Radio-frequency interference

CHAPTER 5: Power disturbances as EMI problems

CHAPTER 6: Circuit boards... bulletproof yours against EMI

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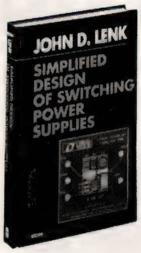

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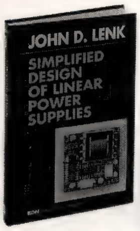

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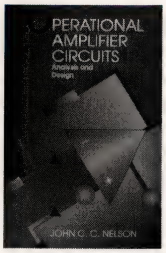

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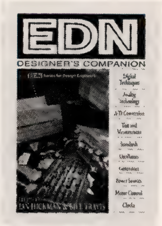

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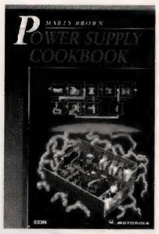

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## Correction

We listed an incorrect phone number for Texas Instruments in the "For free information" box on pg 82 in "Bridge chips help connect host and expansion buses to the PCI bus" (*EDN*, Feb 2, 1995, pg 77). The correct phone number is (800) 477-8924, ext 4500.

---

## Jim Williams' features continue to draw reader response

Jim Williams' article "Be it ever so high-tech, there's no place like home" (*EDN*, Jan 5, 1995, pg 103) and Dennis Feucht's letter in "Signals & Noise" (March 16, 1995, pg 25) should have unequivocally stated that creative engineers who can develop state-of-the-art hardware or software on their own should work primarily for themselves. The home lab should never become a permanent extension of the workday job experience, nor should its fruits be freely given to employers with whom the engineer has no equity position.

Feucht has apparently come to this reality via the backdoor, now that mainstream technology companies are no longer interested in taking advantage of him. However, Williams is seriously shortchanging himself under what I call the "work-is-its-own-reward" theory of career management. Time spent as an employee should not be squandered exchanging excellent and (perhaps) patentable ideas for a paycheck and a pat on the back.

Hasn't Williams looked around and noticed few (if any) engineers aged 50 or 60 working alongside him at the office? Departure from the job (coerced or otherwise) is not all bad—if it is expected or planned. Engineers, though groomed to serve as employees, should grab control of their intellectual property. Although quality advice on this subject is extremely scarce, a good deal on a 1964 Tektronix oscilloscope is no workaround for anger, denial, and today's wonderful euphemism, the "involuntary career change."

*Don Mennie, Technical Writer*
*Mendham, NJ*

I particularly enjoyed Jim Williams' article "Be it ever so high-tech, there's no place like home" (*EDN*, Jan 5, 1995, pg 103). I agree that my lab is a most prized possession, and, to confirm Jim's assertion, it has been the single most important asset to my career advancement.

Besides being important professionally, my lab is both a refuge and a great recreational tool. My wife can confirm that it would be a close call as to which would go first—my pool table or my lab.

If I had $1500 lying around for a new gadget, unlike Jim, I'd save another $1500 and get a brand-new scope, rather than spending [the money] on a curve tracer. Properly instrumented, your circuit can do the necessary curve tracing...in real time.

But, please, don't kid us. You can't possibly do meaningful work in the place shown in those photos. Straight out of *Better Homes and Gardens*, it's far too neat and tidy. Tell us the truth: How long did it take you to get your lab back to operational condition after the photo session?

*James Hansen, Project Engineer*
*New Boston, NH*

---

## Benefits abound in home labs

I loved Jim Williams' article "Be it ever so high-tech, there's no place like home" (*EDN*, Jan 5, 1995, pg 103). I have had a home lab for 38 years, since I was eight years old. Most of the electronics engineering I know I've learned in my home lab. For doing speculative research, the freedom of a home lab is unsurpassed. The combination of cheap, excellent, older analog instruments; cheap, modern PCs; and cheap or free software is intoxicating.

I am currently studying for a PhD in electrical engineering, with a research interest in high-speed, mixed-signal ICs. I have found my home lab better equipped for analog-circuit experimentation than the labs at my university.

In school, I have learned that it is now possible to design (and have built) standard-cell or full-custom ASICs in small quantities at a cost within reach of my home-lab budget.

Well-loaded 486- and 586-class PCs can easily run Linux, a "copylefted" (free) Unix clone, and large (by PC standards) Unix applications. This opens

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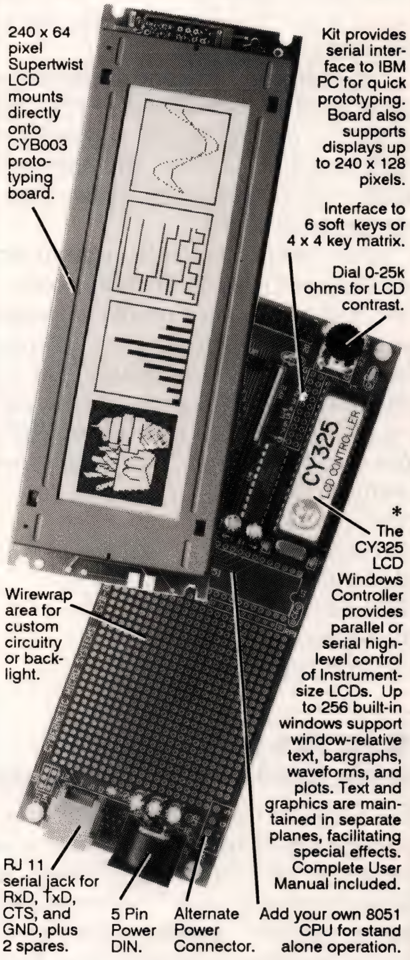
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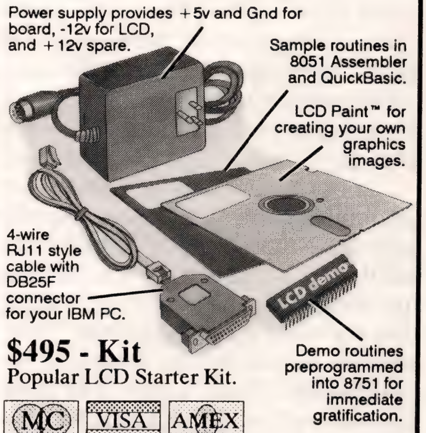
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the way to run free ASIC-design packages, developed at various universities under government grants (our tax dollars at work). See the ads in the *Linux Journal* for more details.

For example, Nascent Technology offers all of the above on CD-ROM for $150 (you pay for the CD and support from Nascent, not for the software itself). You'll find other similar offerings in the *Journal*.

Mosis and Orbit offer fabrication services tailored to small-quantity production. Mosis is oriented primarily toward universities, but it also provides commercial services. Mosis charges universities $750 for fabrication and packaging of 25 pieces of a small custom ASIC. You do all the design, simulation, and testing yourself.

*Peter Anderson,*
*Computer Science &*
*Electrical Engineering,*
*University of Vermont*
*Burlington, VT*
PS: Thanks for Dilbert.

## Tube fan unimpressed with April Fools' write-up

The humor attempt, "Solid-state stereo amplifier emulates tube sound" in your March 30, 1995, issue (pg 22) shows an ignorance that engineers seem to relish. For as long as transistors have been a viable amplifier, engineers have been telling musicians that solid state is equal to or better than tubes. Musicians, unfortunately, were unable to fight the techno-babble with their sense-translated descriptions of sound. Since engineers could not comprehend musicians, they simply derided them.

Carlos Santana told me that my first attempt to make a solid-state amplifier sound like tubes was like "white wine" but that he wanted "red wine." Sensing my confusion, he explained further that my amplifier sounded like "glass" whereas he wanted an amplifier that sounded like "flesh." Later, Al Di Meola told me that my amplifier had no life. These terms are part of the "specifications" customers provide. Their money makes it serious.

Russell Hamm pointed out the behavioral differences in his May, 1973, *Journal of the Audio Engineering Society* paper, "Tubes Versus Transistors—Is There An Audible Difference?" The behavioral differences lie in a region hidden by engineering prejudice. The engineering concepts have very nearly removed warmth from audio. A whole generation of guitar players has been raised on solid-state amps that lack the grace needed for true guitar artistry.

Engineers make amplifiers that are "white wine," "glass," and "dead." They have been doing so for decades because they stick to their prejudices as if they have the same validity as Ohm's law, Thévenin's Equivalences, and Fourier transforms.

*Eric Pritchard*
*Deja Vu Audio*
*Berkeley Springs, WV*

Ed Note: *Most engineers set out to design amplifiers whose outputs are faithful reproductions of their inputs. That is to say, if the source material is a perfectly recorded trumpet or guitar passage, then the amplifier's output should ideally be a bigger version of that passage, with identical amplitude, phase, and harmonic relationships (all objective, measurable parameters, I might add).*

*If this faithful reproduction does not sound "warm" or like "red wine," then the source material did not sound that way, either. If you opt to deliberately introduce various clipping and distortion phenomena in the amplifier to make the sound "warmer," go ahead; it's a free country.*

## More on mixed mezzanines

Your excellent article, "Mezzanine buses bring backplane benefits to the board level" (*EDN*, March 2, 1995, pg 67), correctly points out that the "profusion of competing alternatives has diluted the buses' value." This is true of the myriad proprietary solutions available today. The author concentrates on M-Modules, IP, and PMC, but what must be stressed is that these are precisely the only mezzanines that meet all the criteria for being considered truly open standards: industrial construction, CPU independence, bus independence, nonproprietary specification, wide product range, and multiple vendors (at least five significant manufacturers).

Thanks to the open-standard triad, the price-vs-bandwidth problem is solved: Powerful graphics or network interfaces will be implemented in PMC, whereas simpler I/O functions, fieldbuses, and motor controls will use M-Modules or IP. The mixed PMC and M-Module/IP approach is indeed our position as well as Motorola's. Depending on the application, one may use a high-level mezzanine (PMC), a low-level one (M-Module or IP), or both.

*Michael Tommasi, AART Industries*
*La Seyne, France*

## Williams responds to reader query

Regarding reader JP Browne's comments in "Signals & Noise" (March 30, 1995, pg 27) on P6042 maintenance: There are three choices for replacing custom-IC #M-18.

- It can be quite nicely built up from transistor arrays (see P6042 manual for a schematic of the IC).
- It can be purchased from Deane Kidd (phone (503) 625-7363).
- Its function can be synthesized with a standard off-the-shelf IC with minimal modifications to the P6042 (see Linear Technology Corp's Application Note #61).

And, finally, the above-mentioned Deane Kidd also has a probe cable wire.

*Jim Williams, Staff Scientist*
*Linear Technology Corp*
*Milpitas, CA*

## Hooray for Plug and Play

I read with enthusiasm your article on "Plug and Play" (*EDN*, March 2, 1995, pg 33). Having worked closely with the originating principles of Plug and Play since early 1994, it is refreshing to see positive, honest press on what is a difficult technical challenge, given the large installed base, the restrictive architecture, and the complexities involved. Yet, clearly the goal is worthy and achievable through positive enlightenment of end users. Thank you for your efforts.

I have also been an active contributing member of PCMCIA since 1991. I would like to clarify one point made in your Plug and Play article: The PCMCIA Cardbus is not a 16-bit data path, but a 32-bit data path; it is multiplexed with

*(continued on pg 37)*

**British Rail**

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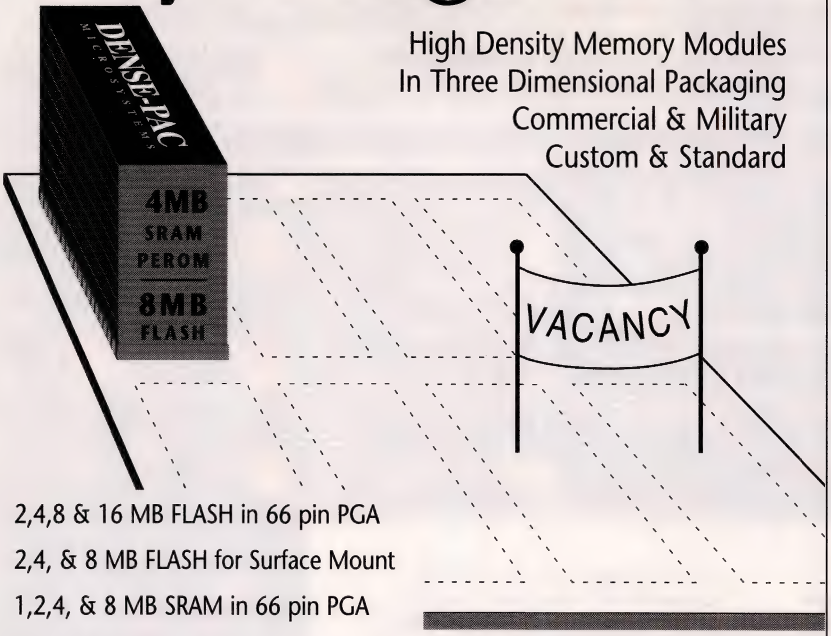

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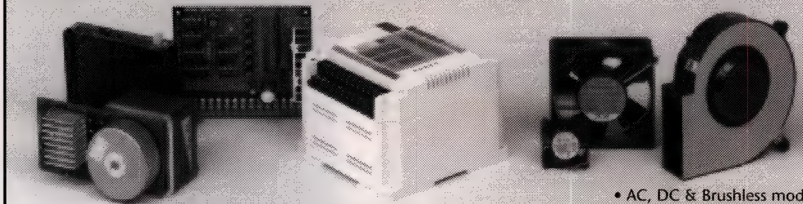

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the address, can run indexed burst mode, and was recently approved to operate at 33 MHz when the appropriate connectors are implemented in a Cardbus-compliant host socket and on the Cardbus-style PC card. Obviously, it is not extensible to the point of the PCI specification, upon which it is based, because the bus can be a 64-bit path, but with only 68 pins in the PCMCIA PC Card interface, the 64-bit option isn't possible in the current definition.

*Tom Geary, Program Manager,*
*Standards Activities*
*Rockwell Telecommunications*

## Clarification of company claim

Regarding "Flurry of engineering software for test, control, and fuzzy design" (*EDN,* Out In Front, March 2, 1995, pg 12), a competitor states that it has "the only product that lets you compare the behavior of systems you design using fuzzy-logic techniques and those you design using classical control theory."

In January 1992, Integrated Systems introduced the RT/Fuzzy modular extension to its $\text{MATRIX}_X$ product family of graphical-modeling, system-design, simulation, code, and documentation-generating tools. The product combines fuzzy-logic reasoning with numerical reasoning for real-time software applications.

For more than three years, the company has been the only provider of fuzzy-logic tools for simulation and modeling. Numerous control-design products have been created for our customers using fuzzy-logic techniques and classical control theory.

*Moses Joseph, VP of Marketing*
*Integrated Systems Inc*
*Santa Clara, CA*

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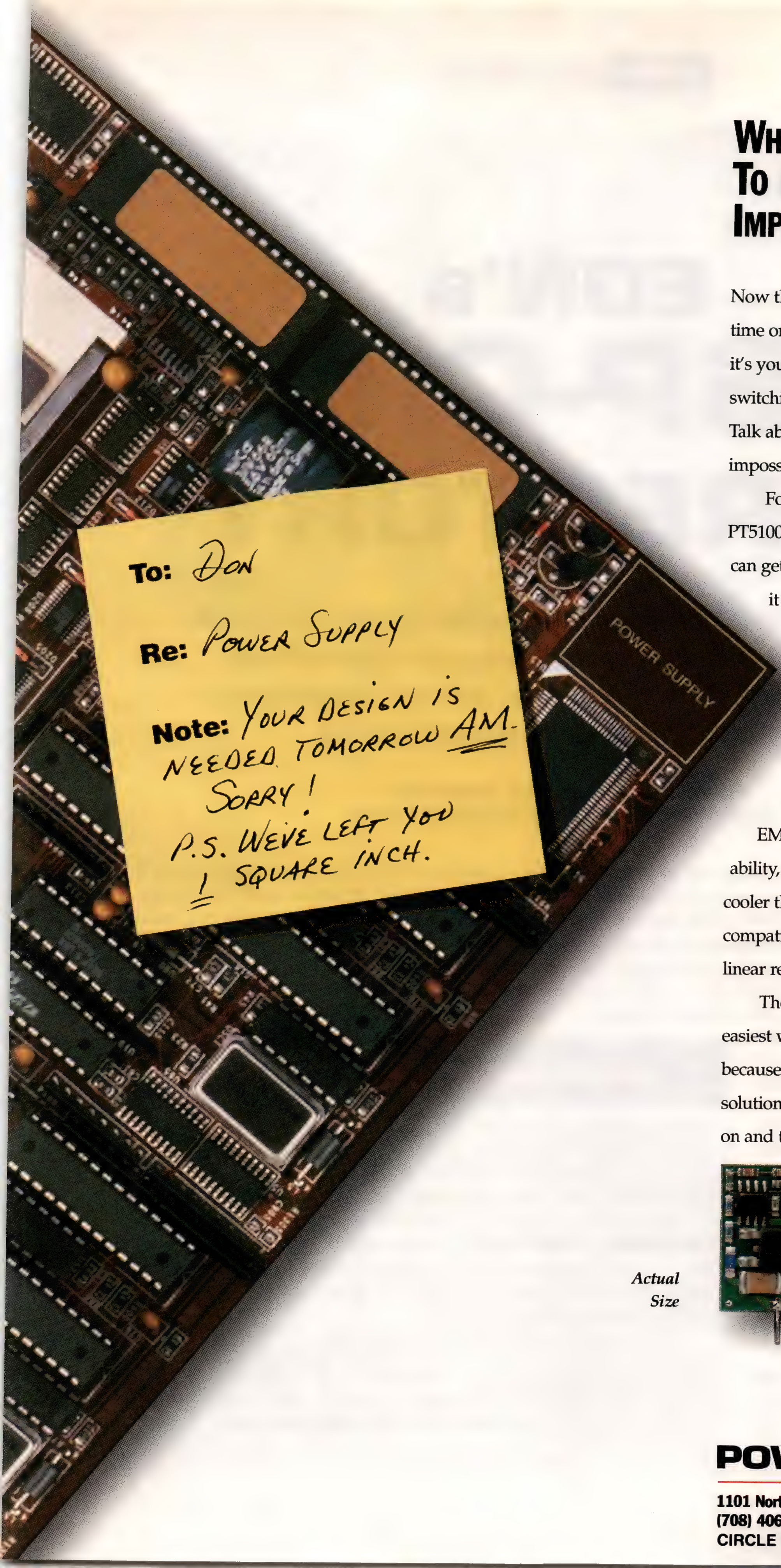
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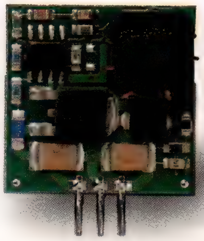
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# EDN's DSP-CHIP DIRECTORY

### Originally, DSP chips targeted niche applications, but today these devices are common in high-volume applications such as modems, cellular telephones, digital audio, and image processing.

*MARKUS LEVY, TECHNICAL EDITOR AND*
*JAMES P LEONARD, SENIOR ASSOCIATE EDITOR*

**Welcome** to *EDN*'s 1995 DSP directory. The goal of this directory is to provide you with concise, useful, and up-to-date information on the general-purpose DSP chips available for your next design. Although your investigation may take you beyond the scope of this directory, use it as a starting point: You'll benefit from 21 pages of comprehensive technical analysis as well as overviews of DSP-chip features and specs.

The DSP devices highlighted in this year's directory are general-purpose processors. Although some of the chips have application-specific features, such as IBM's Mwave DSP with built-in Sound Blaster support, all are reprogrammable and have flexible architectures. And, most of these devices are supported by a range of development tools (see **box**, "Analyzing DSP-development tools").

When comparing different DSP architectures, note how DSP manufacturers choose to optimize their products. In many DSP applications, it's important to move instructions and data around inside the CPU as quickly as possible. To accomplish this, some devices, such as Motorola's DSP96002, have taken the Harvard architecture to the extreme by using as many as eight internal buses, while others, such as AT&T's DSP32C, have limited the number of internal buses to two, thereby optimizing device cost. In addition, some DSPs place an emphasis on fast context switching and, therefore, include multiple register sets; and others still depend on an accumulator-based architecture.

One of the most exciting DSP products introduced this

## ANALYZING DSP-DEVELOPMENT TOOLS

Not only should you analyze a device's performance specs and features, but also take some time to consider the type and quality of development tools and technical support a DSP vendor offers to back its products (including third-party tools). The availability of excellent tools is the most critical aspect of getting your product to market in the shortest time. *EDN*'s DSP directory highlights this subject in the **HARDWARE** and **SOFTWARE** support sections you'll find at the bottom of each page. A quick perusal of Berkeley Design Technologies' 1200-page report, *DSP Design Tools and Methodologies,* proves that there's quite a bit of information available to help you deliberate this issue.

The three-volume set's price tag of $3850 may not fit everyone's budget. But, when you compare this price with the cost of purchasing an expensive development tool and discovering that it falls short of your expectations, it may turn out to be a good investment. For more information, contact Berkeley Design Technologies (Fremont, CA) at (510) 791-9100. **Circle No. 321**

**PHOTOGRAPH COURTESY ANALOG DEVICES**

year is the Texas Instruments TMS320C32, which is the first floating-point DSP to cost less than $10 (250,000). This price breakthrough allows DSP-application designers to take advantage of floating-point-processor performance and ease of use. The TMS320C32 also has a flexible memory interface, allowing connection to 8-, 16-, and 32-bit-wide memories.

Looking ahead to 1996, watch for the debut of new architectures. Philips Semiconductor (Sunnyvale, CA, (408) 991-3838) plans to introduce a programmable-architecture device based on very-long-instruction-word (VLIW) technology. Using VLIW technology, multiple operations can be compounded into a single instruction. Typically, VLIW requires very wide external buses to get instructions into the CPU, which, in turn, raises the cost. The most interesting aspect of Philips' architecture, named TriMedia, stems from the company's patented technology that allows development of this wide-word-based machine without having die-size impact. As a multiple-operation instruction enters the CPU, decode logic distributes each suboperation to one of 27 separate functional units within the core. TriMedia, targeting PC-based multimedia, will sell for less than $50.

# AT-A-GLANCE DSP-CHIP RUNDOWN

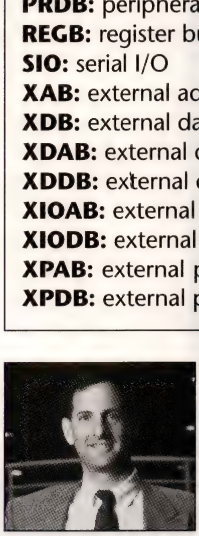
| Vendor | Device | Type | Instruction/ data width | Accumulator width | Barrel shifter/ number of bits | Multiprocessor support | Host interface port | Instruction cache | Hardware stack levels |
|---|---|---|---|---|---|---|---|---|---|
| **Analog Devices**<br>Norwood, MA<br>(617) 329-4700<br>Application Hotline<br>(617) 461-3672<br>BBS (617) 461-4258<br>**Circle No. 310** | ADSP-2100 | 16-bit fixed | 24/16 | 40 | 32 | No | Parallel | 16×24-bit | 16 |
| | ADSP-21020 | 32-bit floating | 48/40 | 80 | 32 | No | No | 32x48-bit | 30 |
| | ADSP-2106x | 32-bit floating | 48/40 | 40 | 32 | Yes | Parallel | 32x48-bit | 30 |
| **AT&T**<br>Allentown, PA<br>(800) 372-2447<br>BBS (610) 712-3771<br>**Circle No. 311** | DSP16xx | 16-bit fixed | 16/16 | 36 | 36 | No | Serial | 15x16-bit | None |
| | DSP32C/ 32xx | 32-bit floating | 32/32 | 40 | 32 | No | Yes, direct to 680x0 or x86 | No | None |
| **DSP Group**<br>Santa Clara, CA<br>(408) 986-4315<br>**Circle No. 312** | Oak/Pine DSP Core | 16-bit fixed | 16/16 | 36 | 36; Oak only | Yes | Customer option | No | None |
| **IBM Microelectronics**<br>Mt Prospect, IL<br>(800) 426-0181, ext 555<br>**Circle No. 313** | Mwave | 16-bit fixed | 24/16 | 32 | 32 | No | Yes | No | None |
| **Motorola**<br>Austin, TX<br>(512) 891-2030<br>DSP Helpline<br>(512) 891-3230<br>BBS (512) 891-3771<br>**Circle No. 314** | DSP561xx | 16-bit fixed | 16/16 | 40 | None | No | Parallel | No | 15 |
| | DSP56000 | 24-bit fixed | 24/24 | 56 | None | No | Parallel | No | 15 |
| | DSP96002 | 32-bit floating | 32/32 | 96 | None | Yes | Parallel (2) | 1024×32-bit | 15 |
| **NEC**<br>Mountain View, CA<br>(800) 366-9782<br>**Circle No. 315** | μPD77C25 | 16-bit fixed | 24/16 | 16 | None | No | Serial | No | 4 |
| | μPD77017 | 16-bit fixed | 32/16 | 40 | 40 | No | Parallel and serial | No | 15 |
| **SGS-Thomson**<br>Phoenix, AZ<br>(602) 867-6100<br>**Circle No. 316** | D950-CORE | 16-bit fixed | 16/16 | 40 | 40 | Yes | No | No | None |
| **Texas Instruments**<br>Dallas, TX<br>(800) 477-8924, ext 3555<br>Tech Hotline<br>(713) 274-2320<br>BBS (713) 274-2323<br>**Circle No. 317** | TMS-320C1x* | 16-bit fixed | 16/16 | 32 | 16 | No | Parallel support (some versions) | No | 4 (8 for the C16) |
| | TMS-320C2x | 16-bit fixed | 16/16 | 32 | 16 | Yes | No | No | 8 |
| | TMS-320C3x | 32-bit floating | 32/32 | 40 | 32 | Yes | No | 64×32-bit | None |
| | TMS-320C4x | 32-bit floating | 32/32 | 40 | 32 | Yes | No | 128×32-bit | None |
| | TMS-320C5x | 16-bit fixed | 16/16 | 32 | 16 | Yes | Parallel | No | 8 |
| | TMS-32C80 | 32-bit multi-processor | 64/32 | 32 | 32 | Yes | Via Hold/HoldA Handshake | 2 kbytes/DSP, 4 kbytes/RISC μP | No |
| **Zilog**<br>Campbell, CA<br>(408) 370-8000<br>BBS (408) 437-8024<br>**Circle No. 318** | Z893XX | 16-bit fixed | 16/16 | 24 | 24 (fixed function) | No | No | No | 6 |
| **Zoran**<br>Santa Clara, CA<br>(408) 986-1314<br>**Circle No. 319** | ZR38001 | 20-bit fixed | 32/20 | 48 | 48 | No | Serial and parallel | 16×32-bit | None |

**Notes:** N/A = Data not available.
*Microchip Technology Inc (Chandler, AZ) is second-source: (602) 786-7200. **Circle No. 320**

| Looping hardware | JTAG support | External interrupt sources | Maximum interrupt latency (cycles) | Special features |
|---|---|---|---|---|
| Yes | No | 3 | 3 | Algebraic assembly, 4 DMA channels. |
| Yes | Yes | 5 | 4 | Off-chip Harvard Architecture, independent parallel computation units. |
| Yes | Yes | 4 | 3 | 512-kbyte on-chip, dual-port RAM, I/O controller with 10 DMA channels. |
| No | Yes | 2 | 8 | Low power (0.7 mA/MIPS), provides architectural expansion with accelerators. |
| Yes | No | 2 | 3 | Bus master interface, byte address space, IEEE P754 compatibility. |
| Yes | On-chip emulation | Pine-2, Oak-3 | 2 | ASIC core, Viterbi accelerator. |
| No | No | None | 2 | ISA bus and MIDI interfaces, Sound Blaster support, audio codec. |
| Yes | Proprietary | 4 | 12 | |
| Yes | Proprietary | 3 | 6 | On-chip emulation, PLL, timer. |
| Yes | Proprietary | 3 | 12 | On-chip emulation, two 32-bit host interfaces, two 32-bit external memory ports. |
| No | No | 1 | 2 | 1-cycle MAC. |
| Yes | Yes | 4 | 2 | Eight 40-bit general-purpose registers/accumulators, parallel instruction set for single-cycle multifunction operation. |
| Yes | Yes | 1 | 4 | ASIC core. |
| No | No | 2 | 7 | 2-instruction MAC. |
| Yes | No | 3 | 8 | Expanded RAM/ROM (up from 'C1x). |
| Yes | Proprietary | 4 | 12 | Flexible memory interface ('C32). |
| Yes | Yes | 4 | 12 | Communication ports. |
| Yes | Yes | 4 | 12 | JTAG scan-based emulation, parallel logic unit, wide range of RAM and ROM options, static operation. |
| Yes, 3 sets | Yes | 4 | 6 (PP), 200 µP | 4 DSPs and RISC µC, 50 kbytes SRAM, video and DRAM control. |
| No | No | 3 | 4 | Codec interface. |
| Yes, 4 levels | Yes, but no boundary scan | 1 | 9 | Fast FFTs, on-chip ICE with JTAG interface. |

## ACRONYMS & ABBREVIATIONS: A KEY TO DSP SCHEMATICS

**AB:** program-and-data address bus
**ACC:** accumulator
**ADC/DAC:** analog-to-digital and digital-to-analog converter
**ADDR GEN:** address generator
**ALU:** arithmetic logic unit
**BS:** barrel shifter
**CDB:** control data bus
**CM:** cache memory
**CPUB:** CPU bus
**DAB:** data address bus
**DB:** program-and-data data bus
**DDB:** data data bus
**DM:** memory for data only
**DMAAB:** DMA address bus
**DMADB:** DMA data bus
**DMAC:** DMA controller
**FP:** floating point
**FX:** fixed point
**GDB:** global data bus
**IDB:** instruction data bus
**INT:** external interrupt
**MAC:** multiply/accumulate
**PAB:** program address bus
**PDB:** program data bus
**P/DM:** program and data memory
**PIO:** parallel I/O
**PM:** memory for program only
**PPCP:** parallel-processor comm port
**PRAB:** peripheral address bus
**PRDB:** peripheral data bus
**REGB:** register bus
**SIO:** serial I/O
**XAB:** external address bus
**XDB:** external data bus
**XDAB:** external data address bus
**XDDB:** external data data bus
**XIOAB:** external I/O address bus
**XIODB:** external I/O data bus
**XPAB:** external program address bus
**XPDB:** external program data bus



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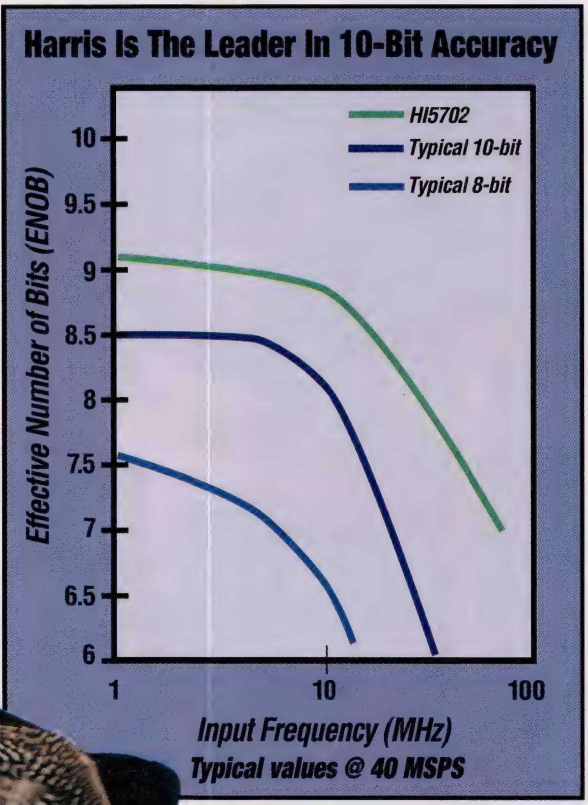

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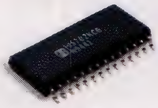

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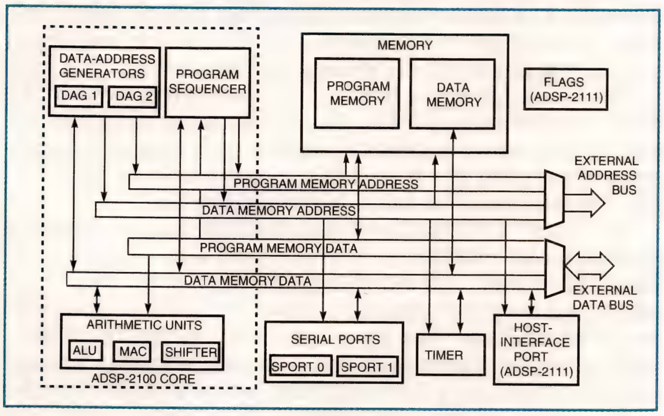
CIRCLE NO. 218

# ANALOG DEVICES ADSP-2100 FAMILY
## 16-BIT FIXED-POINT DSP

## ARCHITECTURE

The ADSP-2100 family's CPU handles general processing needs and delivers single-cycle instruction execution when executing tight DSP algorithms from on-chip memory. Code can execute multiple operations per cycle. The MAC, ALU, and barrel shifter are separate units and can execute in parallel. The registers of each of these execution units are shadowed by secondary registers, allowing fast context switching.



The MAC unit has a 40-bit accumulator (includes 8 guard bits) that can be treated as two 16-bit and one 8-bit register if extended precision is needed when storing results in memory. MAC results must be passed through the ALU to obtain the sign, but this operation can be done in the same instruction cycle as a data store or read. The barrel shifter shifts 16-bit inputs left or right into a 32-bit register. The shifter also includes hardware support for block floating point.

ADSP-2100 family members have two address generators (X and Y) and two buses (program and data). While executing out of the 16-instruction-word on-chip cache, the two buses feed the X and Y data values for each MAC cycle. Thus, program memory can be used as data memory to hold constants for single-cycle MAC processing. The program bus is free for MAC use when the CPU executes out of on-chip program memory. The program memory is dual-ported, which allows two memory accesses in one cycle. For access to external memory, the ADSP-2100 has a programmable wait-state generator for 0 to 7 wait states.

Analog Devices' designers opted for a wide 24-bit instruction word to minimize instruction decoding and speed execution while utilizing complex instruction formats. Data words are 16 bits. The difference in code and data word sizes requires a Harvard architecture with two separate memory spaces. But, Harvard architectures with separate memory spaces are typical for most DSPs; they enable instruction fetches to occur in parallel with single-cycle MAC operations. In the ADSP-2100's case, the different memory sizes can complicate external-memory design.

**Addressing modes**—Immediate, register direct, memory direct, and register indirect. Zero-overhead looping: Each address generator supports up to four loops with three registers each, which define the end, length, and access address. Each generator handles modulo (circular) addressing. One address generator provides bit-reversed addressing (data only).

**Special instructions**—Most instructions are conditional. A DO UNTIL command sets up a sequence of instructions for repeat operations. The hardware has built-in automatic loop control and addressing for MAC processing.

### VARIATIONS.

**ADSP-2101/3**—20 MHz; 70 mA max at 5V (10 MHz; 17.5 mA max at 3.3V for 2103); 2k×24-bit program RAM; 1024×16-bit data RAM; timer; two serial I/Os; 68-pin PLCC. $26 (1000).

**ADSP-2105**—13.8 MHz; 55 mA max at 5V; 1k×24-bit program RAM; 512×16-bit data RAM; timer; one serial I/O; 68-pin PLCC. $9.90 (1000).

**ADSP-2111**—20 MHz; 70 mA max at 5V; 2k×24-bit program RAM; 1k×16-bit data RAM; timer; two serial I/O ports; host-interface port; 100-pin PQFP. $38 (1000).

**ADSP-2115**—20 MHz; 70 mA max at 5V; 1k×24-bit program RAM; 512k×16-bit data RAM; timer; two serial I/O ports; 68-pin PLCC. $13.60 (1000).

**ADSP-2161/2/3/4**—16 MHz; 42 mA max at 5V (10 MHz; 20 mA max at 3.3V for 2162 and 2164); 8k×24-bit program ROM (4k×24-bit for 2163 and 2164); 0.5k×16-bit RAM; timer; two serial I/Os; 68-pin PLCC. The 2161 or 2162, $15.81 (10,000); 2163 or 2164, $9 (10,000).

**ADSP-2165/6**—25 MHz; 60 mA max at 5V (16 MHz; 24 mA max at 3.3V for 2166); 12k×24-bit program ROM; 1k×24-bit program RAM; 4k×16-bit data RAM; timer; two serial I/Os; 80-pin PQFP. $25 (10,000).

**ADSP-2171/2/3**—33 MHz; 76 mA max at 5V (20 MHz; 26 mA max at 3.3V for 2173); 8k×24-bit program ROM (2172); 2k×24-bit program RAM; 2k×16-bit data RAM; 8- or 16-bit host interface; two serial I/O ports; 128-pin PQFP and TQFP. $23 (10,000).

**ADSP-2181/3**—33 MHz; 76 mA max at 5V (33 MHz; 27 mA max at 3.3V for 2183); 16k×24-bit program RAM; 16k×16-bit data RAM; timer; two serial I/O ports; 16-bit internal DMA port to access on-chip memory; 8-bit DMA port to byte memory for program and data-memory transfers; 128-pin PQFP and TQFP. $38/$44 (1000).

**ADSP-21mps58/9**—26 MHz; 95 mA max at 5V; 2k×24-bit program RAM (additional 4k×24-bit program ROM for 21mps59); 2k×16-bit data RAM; timer; two serial ports; host-interface port; 16-bit ADC and DAC; 100-pin TQFP. $26 (10,000).

## SUPPORT

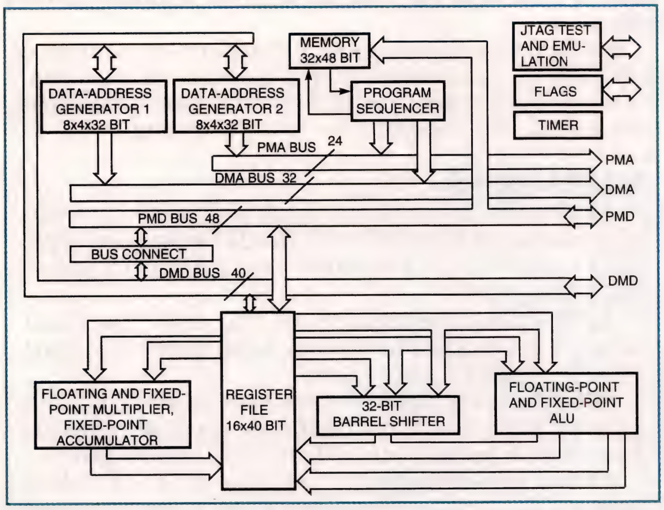
**HARDWARE.** Evaluation boards are available for most ADSP processors. ICEs are available for hardware target debugging.

**SOFTWARE.** Analog Devices supplies an ANSI C compiler as well as an assembler, linker, and interactive simulator.

# ANALOG DEVICES ADSP-21020
# 32-BIT FLOATING-POINT DSP

## ARCHITECTURE

The ADSP-21020, which targets imaging applications, meets IEEE-754 floating-point standards. As with earlier AD chips, the ADSP-21020 takes advantage of a 48-bit instruction word to encode multiple operations per instruction and speed hardware decoding. One detraction, however, is that the large instruction word adds to system cost.



Like the earlier ADSP-2100 16-bit DSPs, the 21020 has no on-chip program or data memory. Instead, the CPU is optimized for executing instructions from a 32-word on-chip cache. The chip also has two external buses with programmable wait states: a 48-bit instruction bus and a 40-bit data bus with 24 and 32 bits of addressing, respectively. The 32-bit 21020 achieves single-cycle MAC execution by executing the inner-loop instructions from its on-chip cache and bringing in the coefficients and data from external memory.

The ADSP-21020 features a Harvard architecture with separate buses for code and data. The buses do not multiplex address information with data or code. Hardware has two address generators to access X-, Y-memory data. Each address generator supports up to four loops with three registers each, which define the end, length, and access address. The ADSP-21020 uses program memory as one of the data memories needed for series evaluation. The program bus and memory provide the X-data-memory values, which combine with the Y-data-memory values for MAC and ALU operations. Although they target high-throughput math processing, AD's DSP processors also have surprisingly sophisticated CPU features. For example, most instructions have conditional execution—they use a preliminary condition test and, if true, then execute the main instruction.

Unlike the early DSP designs, the ADSP-21020 is not a minimal-register, accumulator-based design. Operations center around a 32×40-bit, multiported register file that holds multiple accumulators and registers. For fast context switching, two 16-register segments shadow the register file. The register file serves as the link between the two main buses and the three computational units. The buses pump data into the register file, which unloads to supply input data to the computational units. Ten ports link the computational units and the data and program buses to the register file.

The ADSP-21020's three computational units comprise a floating-point multiplier and fixed-point accumulator, a 32-bit barrel shifter, and a floating- and fixed-point ALU. Each unit is fed from the common register file and returns results to the register file. The three units can operate in parallel, each accessing inputs from and returning results to the register file. Operations are concurrent, unless a conflict results, such as when two units access the same register. Each functional unit executes in a single clock cycle. The ALU flag register holds the results of up to eight ALU compare operations. You can use the accumulated compare flags to implement 2- and 3-D graphical clipping operations.

**Addressing modes**—Immediate, indexed, bit-reversed, circular modulo, register direct and indirect addressing (must use indirect for off-chip memory access).

**Special instructions**—Bit manipulation, division iteration, reciprocal of square root seed, conditional subroutine call, single and block repeat with zero overhead looping, fixed- and floating-point compare, conditional execution. The ADSP-21020 supports IEEE-754 32-bit single-precision floating-point (23-bit data, 8-bit exponent, and sign bit); it can also use 32-bit fixed-point formats, fractional, and integer (2's-complement or unsigned). The PC stack is 20 levels deep. The program sequencer's count and loop stacks are six levels deep and support six levels of interrupt nesting.

### VARIATIONS.

**ADSP-21020**—33 MHz; 500 mA max at 5V; 32-bit timer; no serial ports or DMA; four programmable I/O pins; 223-pin PGA. $124 (1000).

## SUPPORT

**HARDWARE.** Analog Devices sells a full-speed ICE and an evaluation board. Third-party tools are also available. Contact the company for references. The ADSP-21020 includes JTAG support.

**SOFTWARE.** Analog Devices provides a tool set that includes an ANSI C compiler, C compiler with numerical C extensions for math and floating-point applications, source-level debugger, assembler/linker, simulator, application libraries, and PROM splitter. Third-party tools include the Spox real-time OS, filter-design packages, and a graphical application-development package.

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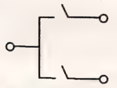

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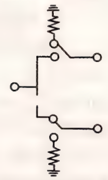

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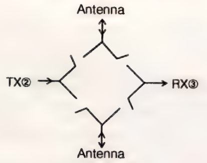

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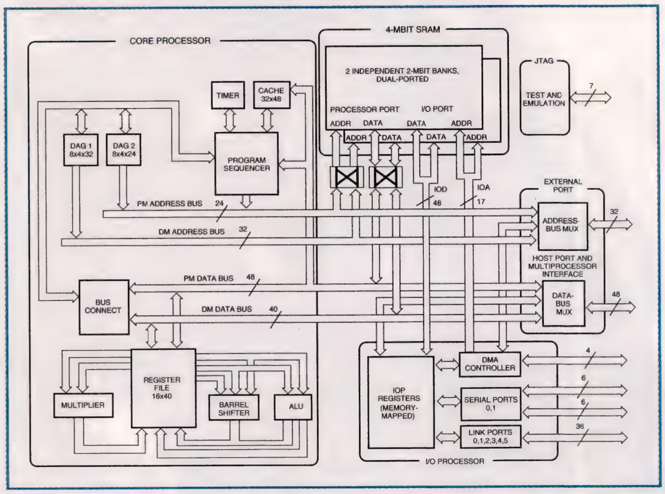
CIRCLE NO. 199

# ANALOG DEVICES SHARC (ADSP-2106X) 32-BIT FLOATING-POINT DSP

## ARCHITECTURE

The Super Harvard Architecture Computer (SHARC) targets communications, speech, sound, graphics, and imaging applications. In addition to the features of the ADSP-21020 32-bit DSP CPU, the ADSP-2106x integrates a large on-chip memory and an I/O controller to offload I/O. This DSP chip has six communication links that enable designers to create DSP multiprocessor meshes; two high-speed serial ports and a host/parallel port that provides a direct interface to off-chip memory, peripherals, a host processor, and bus arbitration for up to six ADSP-2106x chips in a multiprocessor cluster.



The ADSP-2106x's CPU actually executes using only on-chip memory for a range of application code. SHARC contains a 512-kbyte on-chip memory organized into two banks of dual-port RAM that can be combined into 16-, 32-, or 40-bit data and 48-bit instructions. This RAM holds large chunks of critical code and delivers sustained single-cycle memory accesses.

SHARC includes an I/O controller that executes I/O transfers in parallel with CPU execution. The I/O controller offloads reads and writes between on- and off-chip memory—but delays occur when they contend for the same data. The controller manages 10 DMA channels, transferring data among internal memory and external peripheral devices and the host, serial, and link ports. All DMA controller operations are zero-overhead data transfers that generally do not interrupt or delay core thread execution. The synchronous serial ports can deliver transfer rates up to 40 Mbps; the six communication ports move data in 4-bit nibbles, transferring up to 1 byte/clock cycle. With six links operating simultaneously, max throughput is 240 Mbytes/sec.

The CPU, I/O controller, and peripherals interconnect through a multibus-crossbar-interconnection unit that allows flexible, nonintrusive transfers between these units. To reduce bottlenecks, the crossbar permits data and instruction fetches from external or internal memory, cache, and I/O from on- or off-chip peripherals all in a single cycle.

The SHARC provides special communication links or ports. Fed through the I/O controller, these ports enable designers to create meshes of DSP processors. (Each processor in the mesh is defined by point-to-point connections between DSP ports.) The on-chip I/O controller sets up, runs, and responds to these ports. Transfers pass through the I/O ports to and from internal memory. The I/O controller separates these transfers from mainstream DSP.

SHARC has a parallel port that serves as a direct interface to off-chip memory, peripherals, or a host processor. Up to six ADSP-2106x chips can share this bus with a common system processor; the bus implementation includes arbitration. The ADSP-2106x supports page-mode DRAM and fast SRAM external memory. SHARC's address space is unified using a single 32-bit address bus and a single 32- or 48-bit data bus. For a 40-MHz clock, the chip requires a 15-nsec access time for zero-wait-state memory. The special host interface supports both 16- and 32-bit µPs, as well as system buses, such as ISA and PCI. This host is treated as a memory-mapped device, with direct writes or reads to internal memory.

**Addressing modes**—Immediate, indexed, bit-reversed, circular modulo, register direct and indirect addressing (must use indirect for off-chip memory access).

**Special instructions**—Bit manipulation, division iteration, reciprocal of square root seed, conditional subroutine call, single and block repeat with zero overhead looping, fixed- and floating-point compare, conditional execution. SHARC supports IEEE-754 32-bit single-precision floating point (23-bit data, 8-bit exponent, and sign bit) and a 40-bit extended IEEE format for additional accuracy (32-bit data, 8-bit exponent, and sign bit).

### VARIATIONS.

**ADSP-21060/21062**—40 MHz; 720/680 mA max at 5V; 4-/2-Mbit dual-ported SRAM; 32-bit timer; 10 DMA channels; host-processor interface; six link ports for point-to-point connectivity and array multiprocessing; two synchronous serial ports; 240-pin PQFP. $250/$164 (10,000).

## SUPPORT

**HARDWARE.** Analog Devices sells an ICE, which is a full-speed, nonintrusive, JTAG-based emulator that uses the ADSP-2106x built-in debugging capability. It runs under Microsoft Windows and supports debugging for multiple processor systems. Also available is the EZ-Lab Development System, a PC plug-in card for multiple 2106x processors. The ADSP-2106x includes JTAG support. Third-party products include PC and VME multiprocessor cards and operating systems.

**SOFTWARE.** Analog Devices supplies a C compiler that has full support for Numerical C, which extends vector- and matrix-processing capabilities for signal processing. Other tools include an assembler/linker, a simulator, application libraries, a PROM splitter, and a C source-level debugger.

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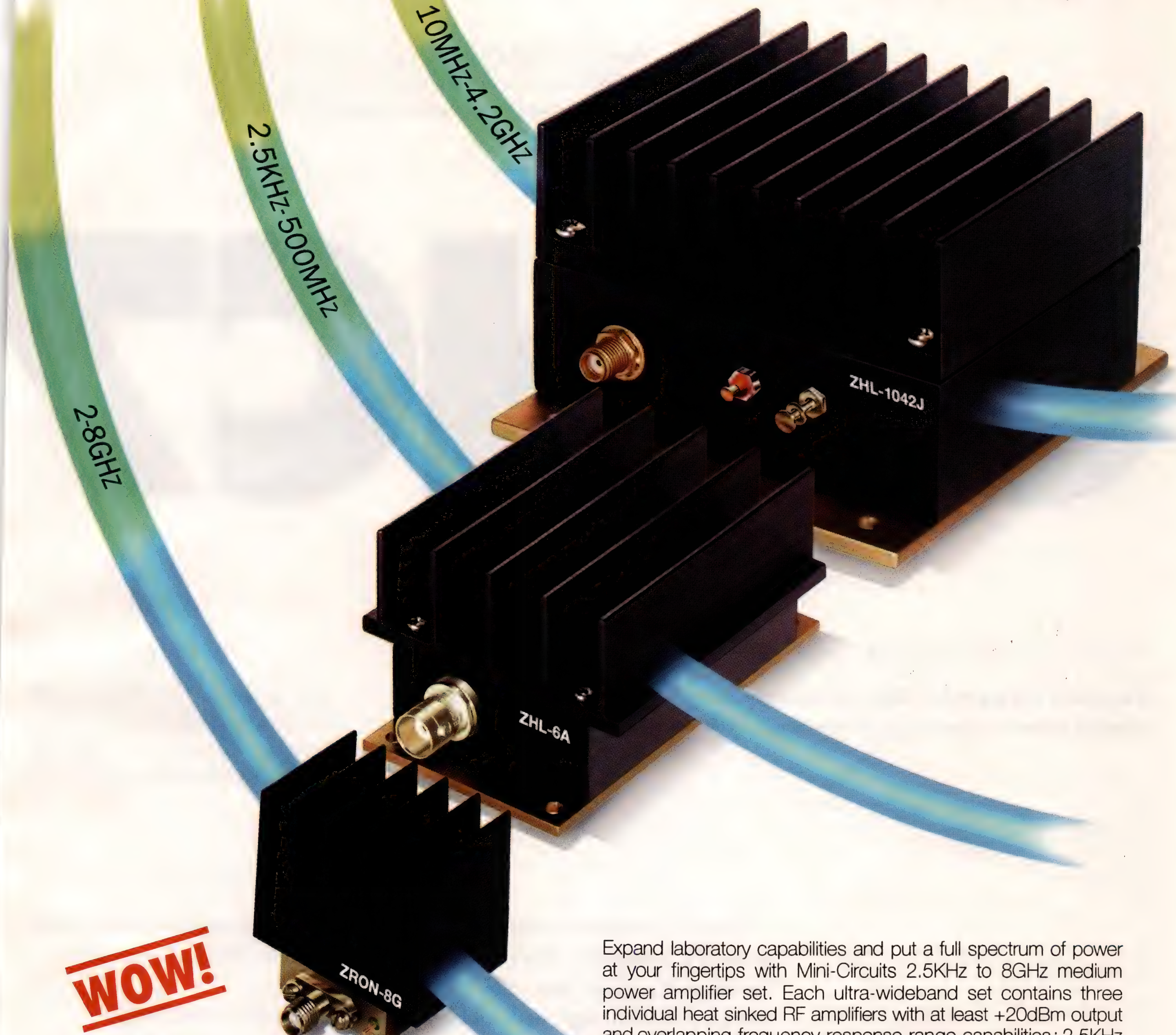

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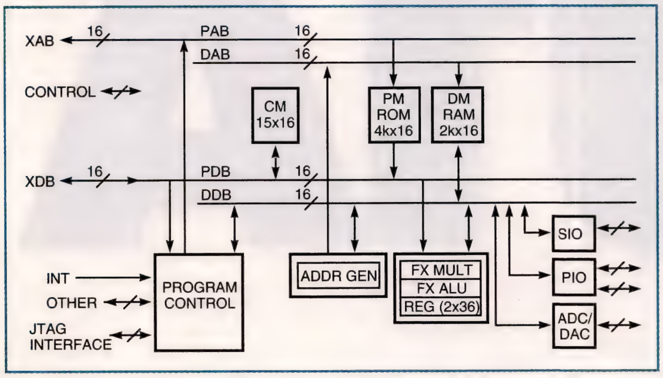
# AT&T DSP16XX FAMILY
# 16-BIT FIXED-POINT DSP

## ARCHITECTURE

The DSP16xx family has a core MAC unit, multiple on-chip memories, a small instruction cache, dual address generators, and multiple buses to move data in parallel. For fast inner-loop processing, an inner-loop code block is loaded under program control into a 15-instruction cache, and the on-chip X and Y memories supply the coefficients and data to drive MAC execution.

The DSP16xx uses three internal buses to move instructions, coefficients, and data in parallel for high-throughput processing. The DSP defines two 64k-word address spaces, one for program/coefficients and one for data. Both X and Y buses connect to the same dual-port RAM. If references to both ports of a single bank occur simultaneously, the chip incurs a one-instruction-cycle penalty and performs data access first. Memory writes always take two cycles.



The DSP has two address-generation arithmetic units: XAAU and YAAU. These units have their own internal adders and registers to hold address values and offsets. The XAAU has a 12-bit adder, 12-bit static offset register, and four 16-bit pointer registers. The YAAU has eight static registers and an adder. Programmers can access XAAU and YAAU registers.

The main execution unit is the data arithmetic unit, which has a 16×16-bit multiplier and a 36-bit ALU/shifter (4 guard bits) with two accumulators. The multiplier and adder operate in parallel, and multiplier inputs and outputs are registered. A full MAC execution is pipelined. In the first stage, the registered inputs drive the multiplier, which outputs a 32-bit result. The MAC can shift the multiply result before running it through the ALU/shifter and into one of the accumulators. The DSP16xx uses fixed-point, 2's-complement arithmetic throughout. The bit-manipulation unit has a 36-bit barrel shifter, two 36-bit accumulators, and four general-purpose 16-bit registers.

## SUPPORT

**HARDWARE.** AT&T supplies a hardware-development system with an ICE pod. Evaluation and demo boards are also available. The DSP16xxs have a JTAG test/emulation port for chip test and in-circuit debugging.

**SOFTWARE.** AT&T sells software-development tools, including a C compiler, assembler/linker, debugger, simulator, and application library.

**Addressing modes**—Register and memory direct, register indirect, immediate; no bit-reversed addressing.

**Special instructions**—Single/block instruction hardware looping; conditional subroutine call; compare; compound addressing; exponent detection; bit-field extract and replace; no rotate instructions. The DSP16xx lacks a hardware stack, complicating subroutine and interrupt nesting.

### VARIATIONS.

**DSP16A**—40 MHz at 5V (25 MHz at 3.3V); up to 32-kbyte ROM; up to 3-kbyte RAM; serial and parallel I/O ports with multiprocessor capability; 84-pin PLCC or PQFP. $15 and $16 (10,000).

**DSP1604/06**—40 MHz; 100 mA typ at 5V (33 MHz; 38 mA typ at 3.3V); 16/24k-word ROM; 1/2k-word dual-port RAM; three 8-bit I/O ports; DRAM controller; JTAG interface; serial I/O ports with optional dual-channel mode; dual crystal oscillator; two timers; low-power modes; 80-pin MQFP, 84-pin PLCC, 100-pin TQFP. $10 to $15.

**DSP1605**—40 MHz; 100 mA typ at 5V; 16k-word ROM; 1k-word dual-port RAM; 8-bit I/O ports; 8-bit parallel host interface; DRAM controller; serial I/O ports with optional dual-channel mode; two timers; dual crystal oscillator; low-power modes; 68-pin PLCC. $10.

**DSP1610**—40 MHz (2× clock option); 130 mA typ at 5V; 512-word boot ROM; 4k- or 8k-word dual-port RAM; sleep mode; bit-manipulation and barrel-shifter unit (BMU); two serial I/O ports; JTAG port; 16-bit timer; four external interrupts; JTAG interface; 132-pin PQFP. $57.

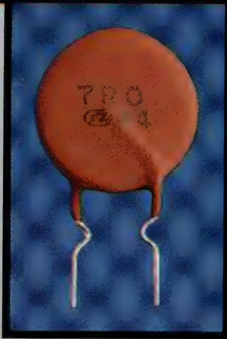
**DSP1611**—100 MHz; 85 mA typ at 5V (26 MHz; 32 mA typ at 2.7V); 2k-word boot ROM; 124k-word dual-port RAM; two serial I/O ports; JTAG port; low-power modes; bit-manipulation and barrel-shifter unit (BMU); timer; two external interrupts; 8-bit parallel host and control I/O interfaces; 100-pin PQFP/TQFP. $61.

**DSP1617**—50 MHz; 100 mA typ at 5V (30 MHz; 32 mA typ at 2.7V); 24k-word ROM; 4k-word dual-port RAM; two serial I/O ports; power-management modes; 5/3/2.7V operation; mask-programmable clock (internal 1 or 2×); 8-bit host and control I/O interfaces; bit/shift unit; JTAG port; 100-pin PQFP/TQFP. $39.

**DSP1618**—50 MHz; 75 mA typ at 5V (30 MHz; 34 mA typ at 2.7V); 16k-word ROM (or 12k-word flash); 4k-word dual-port RAM; two serial I/O ports; power-management modes; 5/3/2.7V operation; mask-programmable clock (internal 1 or 2×); 8-bit host and control I/O interfaces; bit/shift unit; JTAG port; 100-pin PQFP/TQFP. $49.

**DSP1616X30**—50 MHz; 100 mA typ at 5V (30 MHz; 32 mA typ at 2.7V); 12k-word ROM or flash; 4k-word dual-port RAM; two serial I/O ports; power-management modes; 5/3/2.7V operation; mask-programmable clock (internal 1 or 2×); 8-bit host and control I/O interfaces; bit/shift unit; JTAG port; 100-pin PQFP/TQFP. $25.

**DSP1627**—70 MHz; 98 mA typ at 5V (50 MHz; 39 mA typ at 2.7V); 32k-word ROM; 6k-word dual-port RAM; two serial I/O ports; power-management modes (hardware stop=50 μA); mask-programmable clock (internal 1 or 2×); 8-bit host and control I/O interfaces; bit/shift unit; JTAG port; 100-pin PQFP/TQFP. $45 (10,000).



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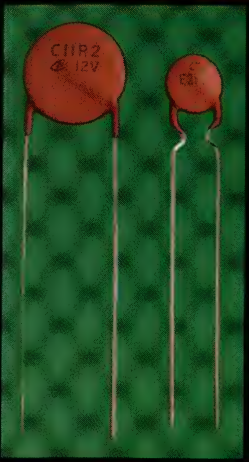

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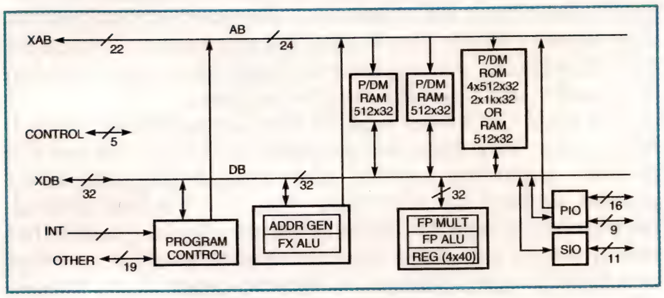
# AT&T DSP32C/32XX FAMILIES 32-BIT FLOATING-POINT DSP

## ARCHITECTURE

The DSP32C is targeted for general-purpose DSP applications. The DSP32xx family, based on the DSP32C, is tailored for PC multimedia, telecommunications, and graphics applications. Instead of relying solely on on-chip memory, the DSP32xx has an on-chip DRAM controller for interfacing to paged-mode DRAM. This interface allows the DSP to share the motherboard's system memory instead of requiring expensive local SRAM for holding code and data. Additionally, the DSP32xx reduces motherboard design-in costs by directly supporting standard μP buses, such as the 680x0 and 80x86 buses.



The DSP32C/32XX has a unique architecture: Rather than using multiple buses to move the instructions and data needed for a single cycle, the DSP's modified Von Neumann architecture handles up to four sequential operations per cycle. The DSP can access up to four 512×32-bit RAM blocks and can drive two core functional units. The CPU has three pipeline stages. Each stage takes four external clocks but performs multiple sequential operations in a given cycle.

The first core functional unit is the data arithmetic unit (DAU), which has a 32×32- to 45-bit floating-point, dedicated, single-cycle MAC unit with four 40-bit accumulators. Only the DSP32xx has a barrel shifter. The second unit is the control arithmetic unit (CAU), which has an integer 16/24-bit ALU and 22 24-bit addressing registers that handle both program and data addressing. (The DSP32xx ALU is 32 bits wide.) The CAU also functions as the address-generation unit when the DSPs are executing a floating-point instruction.

The CAU can generate up to four addresses/cycle, one for each phase or state of an instruction cycle: an instruction fetch, two operand (X,Y) fetches, and a memory write. The DAU is pipelined; it has a four-stage pipeline for a MAC cycle. Thus, the results from a MAC cycle initiated by instruction 1 will be available when instruction 5 starts its first cycle, that is, the fifth cycle from the start of the MAC instruction. The CAU runs in parallel with the DAU; it executes addressing operations as well as control, data-move, and integer ALU operations. The CAU does not include a multiplier; therefore, the DAU must perform integer multiplication and convert results back to integer.

The DSP32xx has two 1k-word, on-chip RAM blocks, which can hold data or code, and a small boot ROM. AT&T designed the Visible Cache Operating System (VCOS) in conjunction with the DSP32xx. A minimal OS, the kernel is only 400 bytes. The VCOS kernel resides in on-chip memory along with critical instructions and data. The operating system helps cut costs by letting the DSP32xx use motherboard main memory for caching instructions and data and for external storage.

An integrated, two-channel DMA controller (not the DSP3207) moves data between memory and the DSP32C/32xx's serial I/O buffer. The DMA controller can access internal and external memory. It uses cycle stealing to move data and does not disturb the CPU's execution thread. The controller can be restricted to request DMA cycles only when the DSP32C/32xx processor has ownership of the shared external bus. This strategy ensures that DMA operations won't incur the overhead of bus-master requests.

**Addressing modes**—Immediate, memory direct, register direct, register indirect, bit reversed (on the DSP32xx, this is done by using add-carry reverse instruction), PC relative. Indexing is available, as are postincrement and decrement options for register-indirect addressing.

**Special instructions**—Single and block repeat without nesting capability and noninterruptible (DSP32xx is interruptible), limited bit manipulation, conditionally executed integer arithmetic, integer compare, conversion to IEEE format; go-to loop with counter, and reciprocal of Y seed. A special multiply-accumulate multiplies two operands from memory, accumulates the product with a value in an accumulator, places results in accumulator, and copies one of the operands to a memory location. The processors do not have a dedicated hardware stack.

### VARIATIONS.

**DSP32C**—50 MHz; 225 mA typ at 5V; 1024×32-bit RAM; 4k×32-bit ROM; 24-bit external addressing; programmable wait states (0 to 3); two DMA channels; synchronous serial port, 16-bit parallel port; no timer; 133-pin PGA/164-pin BQFP (bumpered quad flatpack). $70/$57 (10,000).

**DSP3207**—55/66 MHz; 150/282 mA typ at 3.3V; 2k×32-bit RAM; 256×32-bit boot ROM; 32-bit external addressing; programmable wait states (0 to 3); two DMA channels; 32-bit timer; general-purpose, 8-bit I/O port; 132-pin BQFP. $37/$42 (25,000).

**DSP3210**—55/66 MHz; 220/285 mA typ at 5V; 2k×32-bit RAM; 256×32-bit boot ROM; 32-bit external addressing; programmable wait states (0 to 3); two DMA channels; 32-bit timer; synchronous serial port, 16-bit parallel port; general-purpose, 8-bit I/O port; 132-pin BQFP. $42 (10,000).

## SUPPORT

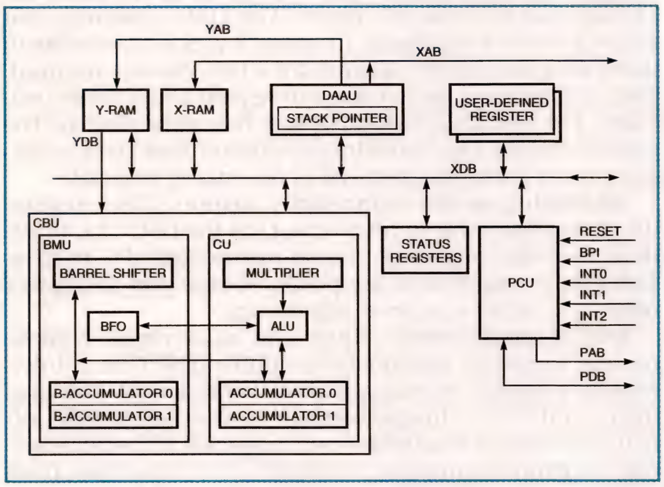
**HARDWARE.** AT&T supplies a development board and an ICE. The DSP32C/DSP32xx devices do not support JTAG. Contact AT&T for references.

**SOFTWARE.** AT&T sells development tools that include a C compiler, assembler/linker, simulator, the VCOS operating system, and a library of multimedia functions.

# DSP GROUP PINE/OAK DSP CORE
# 16-BIT FIXED-POINT DSP ASIC CORE

## ARCHITECTURE

DSP Group developed its own 16-bit DSP core architecture, the Oak DSPCore, and licenses it to developers. Oak is DSP Group's second-generation core, following the Pine core currently available at a number of ASIC vendors. In high volume, Oak- and Pine-based ASICs can cost less than $10 each. These DSP processors are standard cells in many vendors' ASIC libraries. Engineers can make do with the minimal core or, by adding more memory, peripherals, interrupt logic, and custom logic sections, expand the architecture for higher processing efficiencies. At the system level, the chip consists of a 16-bit DSP core with links to on-chip program ROM, data RAM, and a bus-interface unit. The cores use double-metal CMOS technology. Pine is available in 1.0-, 0.8-, and 0.6-μm processes; Oak is available in a 0.6-μm process. Both DSPs have built-in power-management features to cut power dissipation, including 2.7V parts to reduce power consumption further.



Pine has two data buses and one program bus, two RAM data blocks for X and Y memory, a data-arithmetic-address generator unit (DAAU), and a MAC unit. Oak expands on Pine by adding a bit-manipulation unit (BMU), software stack, program-control unit, four optional general-purpose registers, an additional external interrupt, an expanded instruction set, and a special on-chip-emulation module (OCEM) that provides trace and breakpoint capabilities for real-time debugging.

Oak's MAC unit has two 16-bit input registers. The MAC unit takes in two 16-bit numbers, signed or unsigned, and delivers a 32-bit 2's-complement product in one cycle. The product is then sign-extended to 36 bits through 4 guard bits. The ALU performs arithmetic/logical operations on the data operands. It also performs functions such as normalization, step division, and rounding. The BMU has a 36-bit barrel shifter, a bit-field-operation unit, and two additional 36-bit accumulators. The accumulators can rapidly switch context between the two sets of accumulators, including the shadow registers; the accumulators can also evaluate 36-bit exponents. A saturation unit monitors transfers from the accumulators to 16-bit registers or memory and optionally saturates out-of-range values.

At each cycle, the three buses move X and Y memory data to the MAC unit from core X and Y data RAMs while the program-control unit (PCU) fetches a new instruction from on-chip ROM or RAM. The X data bus also serves as the main CPU data bus by linking the two data RAMs, status register, PCU, and a set of general-purpose registers.

The DAAU generates X and Y memory addresses for each MAC cycle and does postoperation modification on the pointers, including modulo addressing. It has nine 16-bit pointer registers for addressing. The core has four general-purpose 16-bit registers, including a top-of-stack pointer that references the top of the current software stack for interrupt or subroutine-processing calls. You can define four additional general-purpose registers that are on the chip but not part of the DSP core. These registers can be handy for application-specific hardware.

Oak supports DMA operation, downloading capabilities from data memory space to program memory space, an automatic boot procedure, and support for two 64k-word address spaces: The X and Y data space and the program space. The X RAM space can be in both internal and external memory; the Y RAM space is in core internal memory only. The X and Y memories can be expanded internally in the core to 2k words, but only the X memory expands externally to 62k words. This potentially limits the performance of certain applications that require simultaneous access of both X and Y memory. The off-core program memory can expand to 64k words. Oak has a built-in 16-bit loop counter for repeating instructions or instruction blocks up to 64k times. A repeat instruction can be nested in a loop block, with up to four levels of block nesting. Oak adds a hardware stack that replaces Pine's software stack; the optional general-purpose registers expand to eight.

**Addressing modes**—direct, register indirect, relative, and index and immediate.

**Special instructions**—conditional subroutine call/return from a subroutine, repeat, division step, bit field test (Oak only), compare, square, accumulate/subtract previous product, move data/program memory, modify accumulator conditionally, support for double-precision calculations, bit-field operations, exponent evaluation, context switching, min/max calculation, and automatic boot.

## SUPPORT

**HARDWARE.** DSP Group supplies an ICE board and evaluation/development board and on-chip-emulation capabilities; the company also sells a bond-out chip for emulation and debugging.

**SOFTWARE.** Software tools include an assembler/linker, loader, simulator and debugger, a C compiler, and the ASSYST simulator, which enables users to map their customized logic into the tools. All tools run under MS-Windows.

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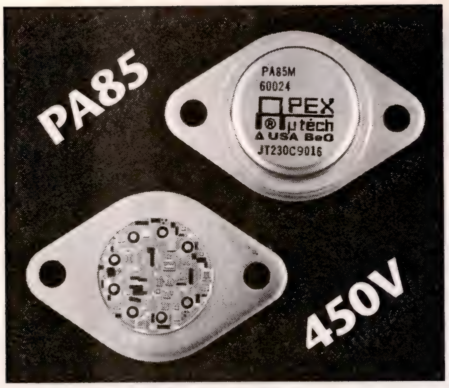

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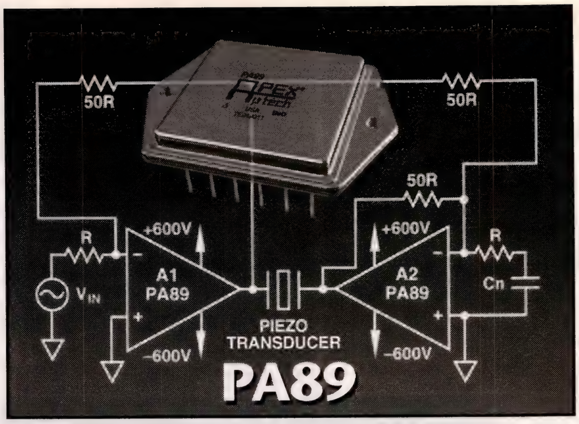

The PA89 is a MOSFET amplifier designed for supply voltages up to ±600V (1200V rail-to-rail). Output current is rated at 75mA with no second breakdown limitations and current limit can be set with an external resistor. Other specifications include 3kHz power bandwidth and 6mA quiescent current. Typical applications: piezo motors, scanning tunneling microscopes, lasers, biomedical, and electroluminescent display drives. **For more information or applications assistance, call Apex Microtechnology Corp., Tucson, AZ, 1-800-862-1015 or FAX 520-888-3329** Circle # 28 in US # 29 in Europe

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  —Single Supply (5V to 40V) or
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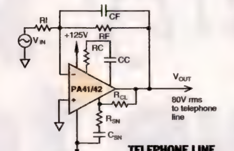
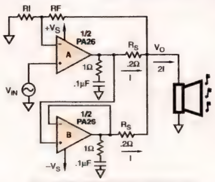
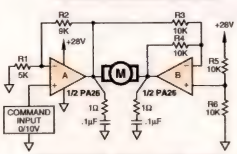
- Wide Common Mode Range
  —Includes Negative Supply
- High Efficiency, Low Distortion



TELEPHONE LINE RING GENERATOR



5A AUDIO PARALLEL CONNECTION



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**KEY FEATURES/KEY SPECIFICATIONS**

| Part # | $V_{SS}$ | $I_O$ | $V_{CM}$ | $V_{SAT}$ | PKG | $/10K |
|---|---|---|---|---|---|---|
| PA26 | 5V-40V | 2.5A x 2 | $-V_S$–.3V | 1.8V @ 1.0A | SIP[1] | $3.45 |
| PA21M[2] | 5V-40V | 2.5A x 2 | $-V_S$–.3V | 3.5V @ 2.A | TO-3[1] | $43.85 |
| PA42 | 100V-350V | 120mA | $\pm V_S$–12V | 10V @ 40mA | SIP[1] | $17.90 |
| PA43 | 100V-350V | 120mA | $\pm V_S$–12V | 10V @ 40mA | SMT | $13.60 |

[1] The TO-3 is a hermetic package; the SIP is a non-hermetic package
[2] "M" designates hi-rel military grade

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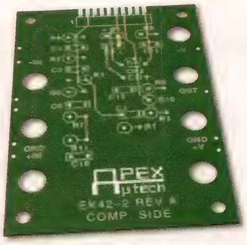
Information on the **PA26, PA42, PA21M** and **PA43** is included in the 6th edition *Apex DC/DC Converters, Power and HV Amplifiers* data book. Call today for your free copy. **1-800-862-1015.**



**Ask about evaluation boards for both the PA26 and PA42.**

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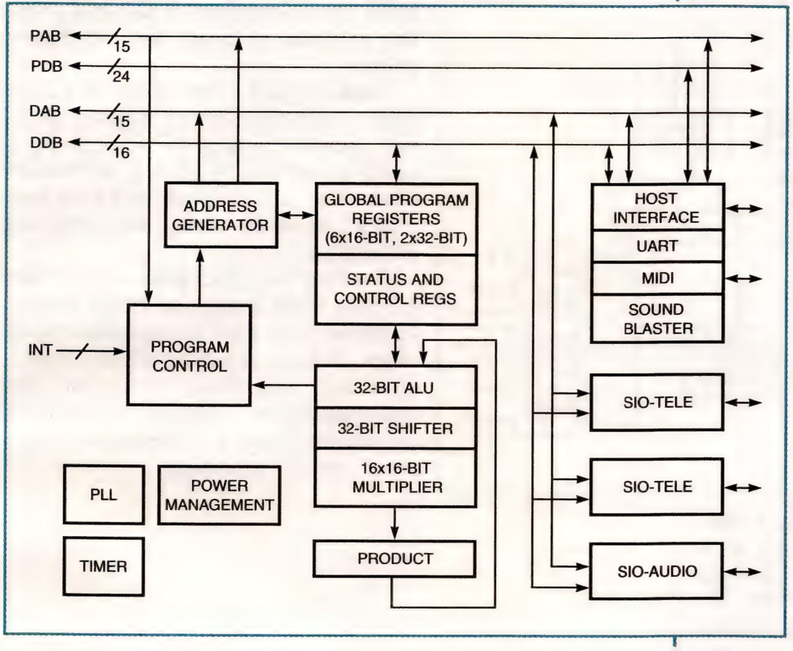
Circle # 32 in US # 33 in Europe

# IBM MWAVE FAMILY
# 16-BIT FIXED-POINT DSP

## ARCHITECTURE

The Mwave family, targeted strictly for PC-based telephony and multimedia applications, features on-chip peripherals for connecting to the ISA bus and a MIDI interface, on-chip support for Sound Blaster, and direct control of audio and telephony codecs. Current-generation DSPs are not intended for embedded or high-speed DSP applications (future chips will address these applications). IBM's Mwave can access 64 kbytes of memory (32-kbyte instruction and 32-kbyte data), and additional memory may be accessed using the DSP's ISA bus and DMA interfaces.



Mwave's core features a three-stage pipeline with a 16×16-bit multiplier, a 32-bit accumulator, a 32-bit ALU, and a 32-bit barrel shifter. Although the processor lacks guard bits, it performs saturation, rounding, and single-cycle min/max functions. Mwave has eight general-purpose registers, including two 32-bit accumulators that allow concurrent operation on two data points. The two accumulators may be employed to calculate two results per loop iteration, making double use of a single coefficient fetch. Using a Harvard architecture, Mwave's separate program and data memory spaces are accessed via 24- and 16-bit-wide buses, respectively.

The host-bus interface features a DMA bus master, which allows the DSP to bring a segment of PC system memory into the DSP-accessible memories at speeds up to 3 Mbytes/sec. The host bus interface also provides Sound Blaster support and UART and MPU401 MIDI register decodes. Although the current implementation only supports ISA, future versions will support PCI to provide higher bandwidth.

The audio-codec interface supports connection to Crystal Semiconductor's CS4215, CS4216, and CS4218 stereo-audio codecs. The telephony codec interfaces connect to TI's TLC32046 AIC chips, TCM320AC36 voice-band audio processors, and TP3054B μ-Law codecs. Depending on the set of codecs used, some of the chip I/O can be reallocated to provide parallel-port capabilities.

**Addressing modes**—Indexed, base, immediate, circular modulo, program counter relative.

**Special instructions**—Bit manipulation, log base 2, many types of compare instructions. Mwave does not support conditional execution or hardware looping for single and block repeat; it also has no hardware stack.

### VARIATIONS.

**MDSP2780**—25 MHz; 126 mA max at 3.3V; timer; power management; PLLs create 17-, 20-, and 25-MHz clocks; 240-pin QFP. $24.60 (10,000).

## SUPPORT

**HARDWARE.** IBM Mwave provides a reference design kit for qualified accounts that includes a prototype adapter card, system software, design specifications, and Windows-based application examples. Mwave's lack of a JTAG port is not critical because the PC is used as the development platform.

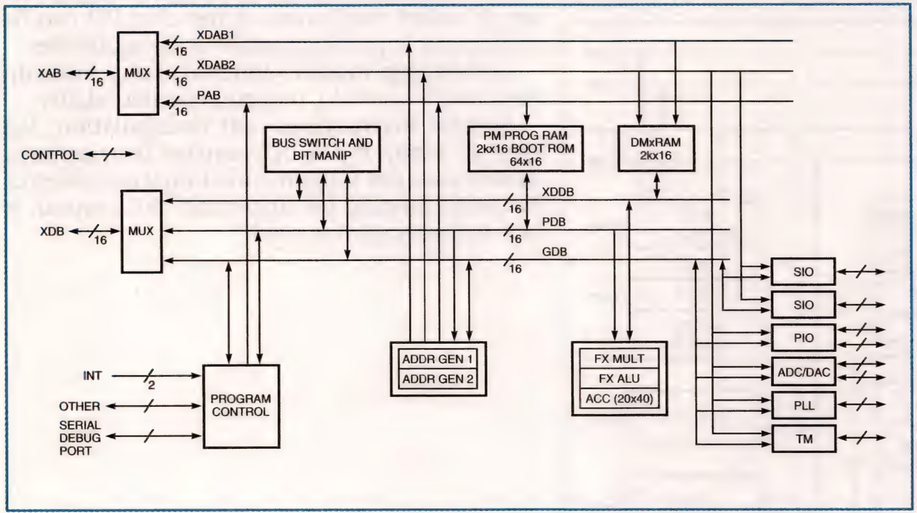
**SOFTWARE.** IBM sells an Mwave developer's kit that includes an ANSI compiler, assembler, linker, and real-time debugger with software oscilloscope signal display for Windows and OS/2.

# MOTOROLA DSP561XX FAMILY
# 16-BIT FIXED-POINT DSP

## ARCHITECTURE

Motorola's 16-bit DSP561xx processors build on the basic DSP56000 architecture, adding a codec for D/A and A/D voice conversions for digital-cellular and voice communications. The DSP56156 suits the European cellular standards; the DSP56166 suits the emerging American and Japanese VSELP standards.

The DSP561xx delivers single-cycle (two-clock) MAC operation and offers hardware support for sum of products and vector processing. Like the DSP56000, the DSP56156/166 is partly an accumulator-based architecture and partly a register-based machine. The core MAC unit has two 40-bit accumulators (includes eight guard bits) with four 16-bit input registers to hold incoming variables and coefficients. The input registers must be loaded prior to the MAC instruction. You can load the MAC input registers in parallel with the MAC operation. When storing results to 16-bit memory, limiter circuitry optionally saturates the 40-bit accumulator values to ±1.0. The DSP561xx lacks a barrel shifter.



The DSP561xx has on-chip program RAM and dual-ported data RAM; each has its own address and data bus. The dual-ported data RAM allows the address generator to deliver two addresses per pipeline cycle, yielding two data reads or one read and one write. The address generator has twelve 16-bit registers (address, offset, and modification) for sophisticated addressing and holding interim data values. The address-generator registers are accessible via a global data bus that links the address-generator registers to external memory, peripherals, and a bit-manipulation functional unit.

The chip's 16-bit external bus multiplexes between 64-kbyte program and data memories. The CPU can perform a single access to external memory with no instruction-cycle penalty, but when using slower memory, wait states may be requested externally or controlled programmably. With a 60-MHz external clock and a 30-MHz basic pipeline cycle, a CPU memory fetch must take less than 33 nsec for single-cycle execution. For MAC processing, portions of the X-memory space supply Y-memory values. The DSP561xx has two data-memory address buses that fetch data from the X-memory RAM and from the external memory for Y-memory values.

**Addressing modes**—Register direct, memory direct, register indirect (postincrement/decrement by 1 or offset indexed by offset), and immediate. The address generator also supports modulo and bit-reversed addressing.

**Special instructions**—Hardware looping with single and block repeat; conditionally exit instruction block loop, division iteration, double-precision multiply step instruction, bit manipulation, compare. DSP561xx processors have a 15-level hardware stack useful for nesting.

### VARIATIONS.

**DSP56156**—60/40 MHz; 188 mA max at 5V; 4-kbyte program RAM; 4-kbyte data RAM; 128-byte boot ROM; 8-bit host processor interface; timer; codec; two serial I/O ports; 27 I/O pins; 112-pin CQFP. $46.10/$44.10 (1000).

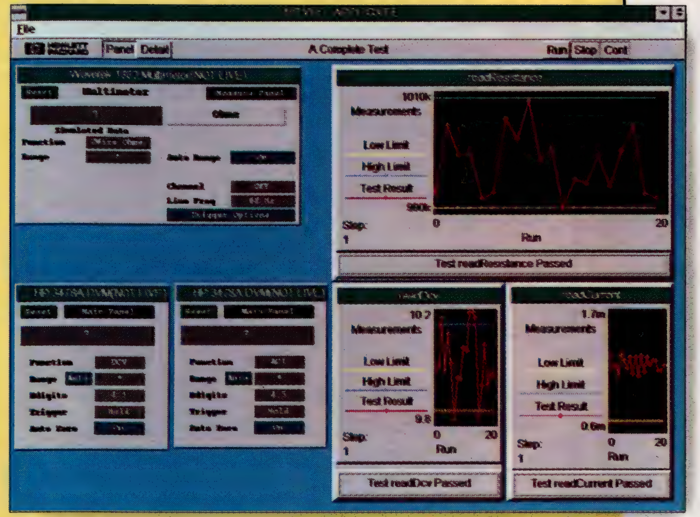
**DSP56166**—60 MHz; 100 mA max at 5V; 4-kbyte program RAM; 8-kbyte data RAM; 128-byte boot ROM; 8-bit host-processor interface; timer; codec; two serial I/O ports; 25 I/O pins; 112-pin CQFP. $51.21 (1000).

## SUPPORT

**HARDWARE.** Motorola fields the Application Development System with ICE operation using the DSP's on-chip emulation features. The on-chip emulator port lets external hardware set breakpoints, single-step, and read/modify memory or registers. You can configure the chip to run with external RAM for development. Third-party tools are also available. Contact Motorola for references.

**SOFTWARE.** Motorola supplies a Gnu C compiler and debugger, assembler/linker, and simulator. Third-party vendors supply data-acquisition and filter-design packages as well as operating-system software. Contact Motorola for references.

# When it is time to switch to graphical test programming, make sure the language you choose won't force you to change everything you've done in the past.



Test readResistance Passed

Test readDcv Passed

Test readCurrent Passed

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CIRCLE NO. 187

**TOKIN TECHNOLOGY UPDATE**

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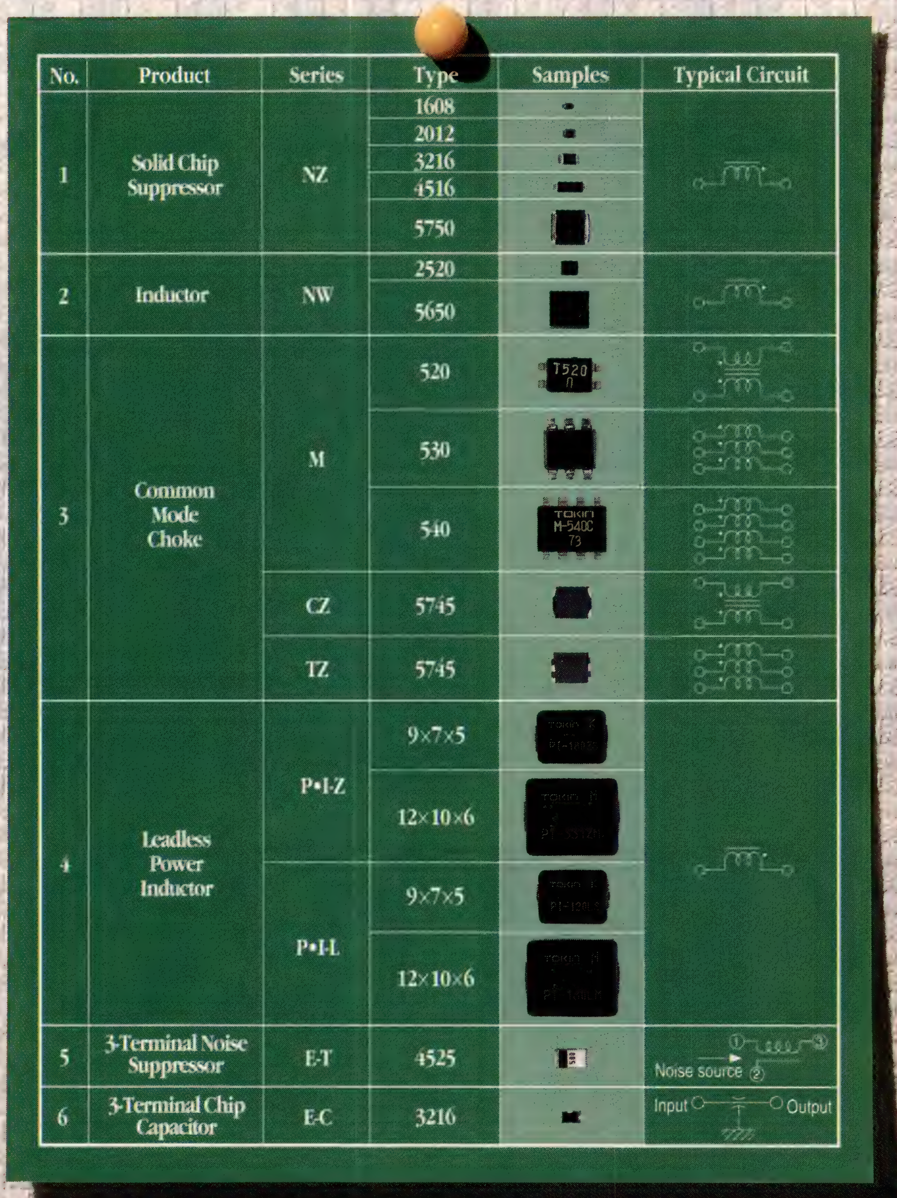
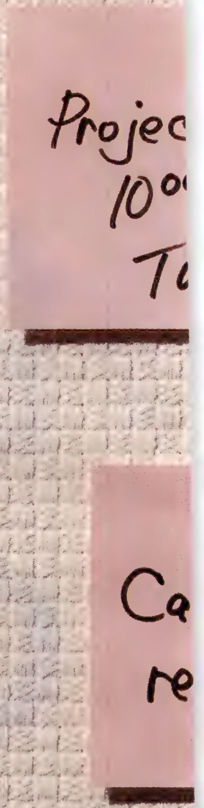


| No. | Product | Series | Type | Samples | Typical Circuit |
|---|---|---|---|---|---|
| 1 | Solid Chip Suppressor | NZ | 1608 | | |
| | | | 2012 | | |
| | | | 3216 | | |
| | | | 4516 | | |
| | | | 5750 | | |
| 2 | Inductor | NW | 2520 | | |
| | | | 5650 | | |
| 3 | Common Mode Choke | M | 520 | | |
| | | | 530 | | |
| | | | 540 | | |
| | | CZ | 5745 | | |
| | | TZ | 5745 | | |
| 4 | Leadless Power Inductor | P•I-Z | 9×7×5 | | |
| | | | 12×10×6 | | |
| | | P•I-L | 9×7×5 | | |
| | | | 12×10×6 | | |
| 5 | 3-Terminal Noise Suppressor | E-T | 4525 | | ① ③<br>Noise source ② |
| 6 | 3-Terminal Chip Capacitor | E-C | 3216 | | Input Output |



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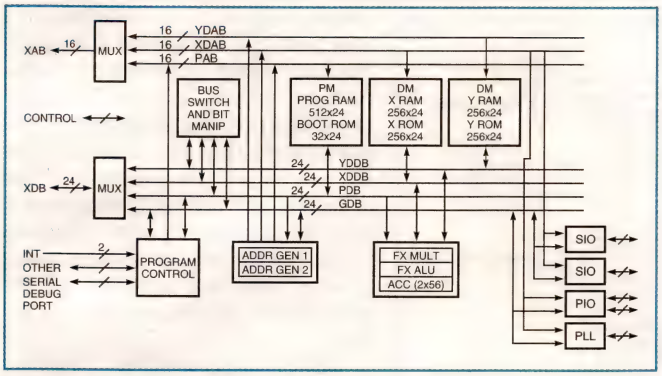
**CIRCLE NO. 185**

# MOTOROLA DSP56000 FAMILY
# 24-BIT FIXED-POINT DSP

## ARCHITECTURE

The DSP56000 targets audio and other applications that take advantage of the larger data size. The processor integrates μC buses and architectural concepts with a DSP MAC core and X and Y memory blocks. Thus, unlike many early fixed-point DSPs, the DSP56000 has a versatile external memory bus, standard bit-manipulation capabilities, and the ability to execute directly from external memory with single-cycle accesses. The chip has no on-chip program ROM, except for a small boot ROM on some versions. However, the DSP56000 can access external memory each cycle without any time penalties.



The DSP56000 isn't exactly an accumulator-based machine. It does have a single-cycle MAC unit, but the unit has two 56-bit accumulators (eight guard bits) and is fed by two sets of two 24-bit registers. Data have to be loaded into the MAC registers before being used; however, the MAC takes one cycle (two clocks) for a multiply and an accumulate. Other registers include control and addressing registers. The control registers are memory-mapped, that is, they are discrete but are addressed by memory location.

Like many DSPs, the DSP56000 has two address generators that automatically access X and Y memories for MAC cycles. Each hardware generator has a 56-bit ALU and three sets of four registers: one set of base address registers, one set of offset registers, and one set of modifier registers. The modifier registers can specify the type of address-register arithmetic operation, or they can hold data.

The processor combines 16-bit addressing with 24-bit words. It has three internal address/data bus pairs: X, Y, and program. The three buses allow an instruction fetch and two data accesses in a single cycle and, therefore, avoids the need for an on-chip cache. A fourth bus, the global data bus, is a simple 24-bit logic bus. Any of the internal address and data buses can be switched into the external 16-bit address and 24-bit data bus; external devices can access internal memory via a bus request. When the 56000 stores 56-bit values to 24-bit memory, you can deploy an optional shifter and saturate the value to ±1.0. The DSP56000 supports three 64-kbyte address spaces—one each for X, Y, and program memory. Unlike many DSPs, the X and Y memories have their own address spaces, which include on-chip RAM and ROM for the bottom addresses. An internal bus-switch unit handles transfers between internal buses. The bit-manipulation unit performs bit operations on memory values and address, control, and data registers.

**Addressing modes**—Register direct, memory direct, register indirect, immediate, and bit-reversed.

**Special instructions**—DO/EndDO, single or block instruction hardware looping, bit manipulation, compare, divide iteration, jump if bit clear/set, jump to subroutine conditionally, move program memory. Logic operations are only performed on bits 24 through 47 of the accumulator. For subroutines, interrupts, and hardware DO loops, the 56000 has a 15-level stack.

### VARIATIONS.

**DSP56002**—40/66 MHz; 90 mA max at 5V; 512×24-bit program RAM; two 256×24-bit data RAMs; 64×24-bit boot ROM; two 256×24-bit data ROMs containing sine, $\log_2$, and $2^x$ tables; 8-bit host-processor interface with DMA support; 24-bit timer; PLL; power-saving modes; synchronous serial interface; serial communication interface; 24 I/O pins. In 132-pin PQFP, $29.37/$39.30; in 144-pin TQFP, $31.13/$41.06.

**DSP56L002**—40 MHz; 50 mA max at 3.3V; 512×24-bit program RAM; two 256×24-bit data RAMs; 64×24-bit boot ROM; two 256×24-bit data ROMs containing sine, A-Law, and μ-Law tables; 8-bit host-processor interface with DMA support; 24-bit timer; PLL; power-saving modes; synchronous serial interface; serial communication interface; 24 I/O pins. In 132-pin PQFP, $34.37; in 144-pin TQFP, $36.13.

**DSP56004**—50/66 MHz; 90 mA max at 5V; 512×24-bit program RAM; two 256×24-bit data RAMs; 32×24-bit boot ROM; two 256×24-bit data ROMs containing sine, A-Law, and μ-Law tables; serial host-processor interface; PLL; power-saving modes; serial audio interface; four general-purpose I/O pins. In 80-pin PQFP, $25.45/$30.50.

**DSP56007**—50 MHz; 90 mA max at 5V; 6400×24-bit program ROM; 3200×24-bit data RAMs; 52×24-bit boot ROM; two 512×24-bit data ROMs containing sine, A-Law, and μ-Law tables; serial host-processor interface; 24-bit timer; PLL; power-saving modes; serial audio interface; four I/O pins. In 80-pin PQFP, $38.

## SUPPORT

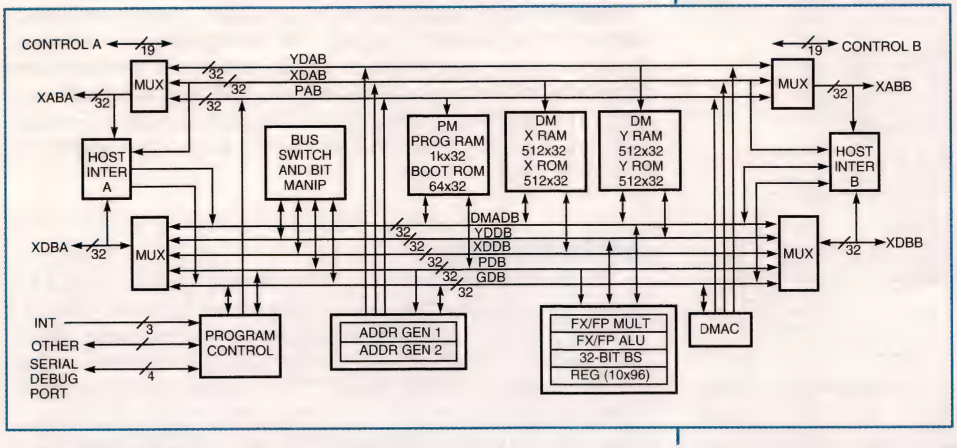
**HARDWARE.** Motorola offers a low-cost DSP56002 evaluation board as well as a 40-MHz application-development system. Third-party hardware tools are available; contact Motorola for references. The 56000 uses a proprietary debug interface (OnCE) in lieu of the standard JTAG interface.

**SOFTWARE.** Motorola supplies a Gnu C compiler and debugger, assembler/linker, and a simulator. Third-party vendors supply data-acquisition and filter-design packages as well as operating-system software. Contact Motorola for references.

# MOTOROLA DSP96002
# 32-BIT FLOATING-POINT DSP

## ARCHITECTURE

Motorola's 32-bit DSP96002 has found a home in high-end DSP and military sockets. Basically a 32-bit floating-point extension of the 24-bit fixed-point DSP56000, the DSP96002 has five major internal buses to speed multiple-operation processing. These buses include program-, X-, and Y-memory bus sets. They also include a global data bus for transferring address and local data and a DMA bus that supports two DMA channels. The on-chip DMA controller moves data without disrupting the DSP CPU's instruction thread.



The DSP96002 also has two 32-bit external bus interfaces with separate address and data buses with page-mode DRAM support. These external interfaces have built-in multimaster capability. Another DSP96002 or a host processor can use a bus request to take over the bus and use it to access shared external memory or the DSP96002's internal memory.

Motorola's DSP96002 presents a programming model nearly identical to that of the earlier 24-bit DSP56000 fixed-point processor. Motorola engineers extended the instruction set with floating-point instructions and extended the registers (including addressing registers) from 16 to 32 bits.

The register-based DSP96002 is built around a multiported register file of 10 96-bit registers. Similar to the DSP56000, the DSP96002 has X and Y RAM and ROM blocks to supply the coefficients and variables for sum-of-product MAC calculations. MAC operations take input data from the register file, so, although MAC operations aren't pipelined, the X, Y data accesses must be pipelined to pump data into the register file before the downstream MAC operation uses the data.

Execution units include a separate multiplier, adder/subtracter (handles both add and subtract for FFT calculations), logic unit, and barrel shifter. These units support integer operations as well as floating-point operations with 11-bit exponents and 32-bit mantissas. The DSP96002 meets IEEE standards for single- and double-precision floating-point representations.

The DSP96002 essentially has the same address-generation unit as the earlier DSP56000. This unit consists of two address generators that can operate concurrently. The generators each have three sets of four 32-bit registers: address (address pointers), offset (offset values), and modify registers. These registers are loaded and accessed via the global data bus. The DSP96002 has a flexible architecture; many typically hardwired features are available as programmable options that you can set up via control registers. For example, the DSP chip supports a mix of address spaces ranging from a single unified address space to one that has separate 32-bit spaces for X, Y, and program memory.

**Addressing modes**—Register direct, memory direct, register indirect (postincrement/decrement by 1 or offset, indexed by offset), and immediate. The address generator also supports modulo and bit-reversed addressing.

**Special instructions**—Hardware looping with single and block repeat, bit test and change, compare graphics, conditional subroutine call and branch, convert integer to floating point (and vice versa), reciprocal seed, reciprocal square root seed. DSP96002 doesn't support conditional execution instructions. For subroutines and interrupts, DSP96002 has a 15-word stack.

### VARIATIONS.

**DSP96002**—33.3/40 MHz; 600 mA max at 5V; 1-kbyte×32-bit program RAM, which can be configured as an instruction cache; two 512×32-bit data RAMs; two 512×32-bit preprogrammed data ROMs containing sine, A-Law, and μ-Law tables; two 8- to 32-bit host ports with DMA support; power-saving modes; timer/event counter; 223-pin PGA. $143/$172.

## SUPPORT

**HARDWARE.** Motorola sells the Applications Development Module for evaluating and debugging the DSP96002. The module uses the processor's on-chip emulation support to set breakpoints, single-step the CPU, and read/modify memory or registers (no JTAG support). You can configure the chip to run with external RAM for development. Some third-party tools are available; contact Motorola for references.

**SOFTWARE.** Motorola supplies a Gnu C compiler and tools as well as an assembler/linker, librarian, application library, and behavioral simulator. Third-party tools include C and Ada compilers, graphical development systems, filter-design software, and real-time operating systems. Contact Motorola for references.

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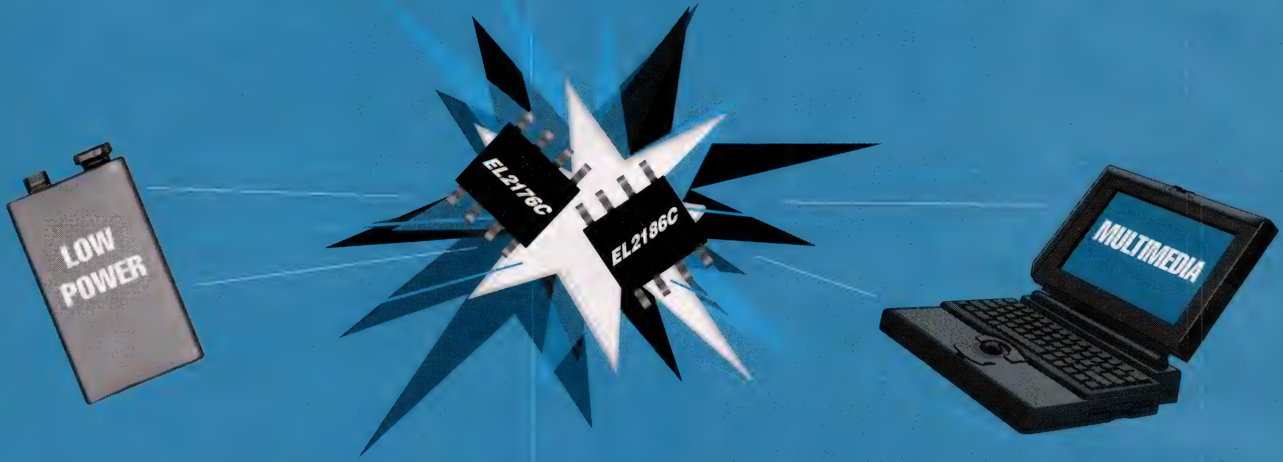

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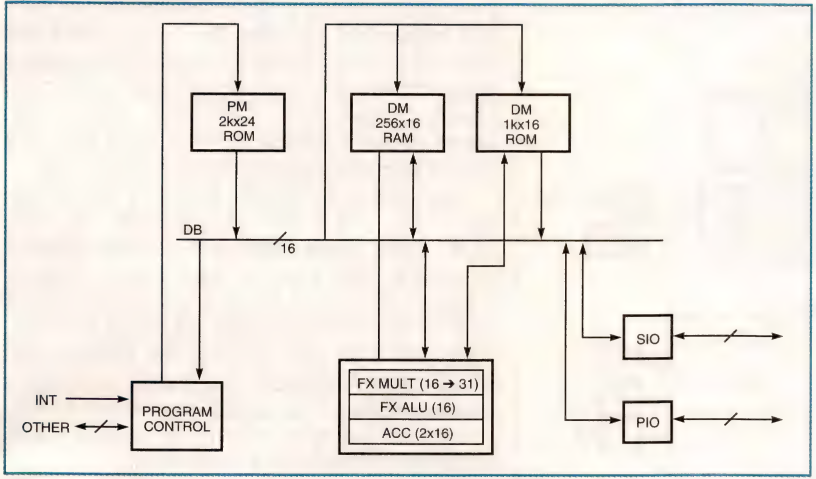
# NEC μPD77C25
# 16-BIT FIXED-POINT DSP

## ARCHITECTURE

The 16-bit fixed-point μPD77C25 has an accumulator-based architecture that is built around a pipelined MAC core and runs from on-chip program and data memory. The C25 has 2048 24-bit instruction words and two data blocks to hold MAC inputs: 512 bytes of data RAM and 2048 bytes of data ROM. Program and data ROM are also available as EPROM or OTP memory. The μPD77C25 handles pipelined, single-cycle MAC operations with a 16×16-bit multiply and a 16-bit accumulate.



The μPD77C25 can run in stand-alone mode or in conjunction with a host processor. It has an 8-bit parallel I/O host port for exchanging data or DSP status with a host processor. This port can interface with standard μC buses such as the 8080, 8085, and 8086 and can handle 8-bit or double-buffered 16-bit data transfers. The μP77C25 also has two serial ports, which can interface to serial peripherals such as ADCs, DACs, codecs, and other μPD77C25 DSPs. You can configure the serial ports for single- or double-byte transfers.

NEC's μPD77C25 has three on-chip memories: one program and one data ROM/EPROM/OTP-memory block as well as a data-RAM block. The CPU can fetch two values per cycle to fill the multiplier input registers while getting the next instruction. The DSP has one 16-bit data bus that links to all memories and peripherals. For MAC data fetches, the RAM bypasses the data bus and directly feeds one of the MAC inputs. The data bus feeds the other MAC input, which passes data from the data ROM/EPROM/OTP-memory block.

The MAC unit is pipelined; the multiplier and accumulator-adder run in parallel. A multiply-accumulate takes two clock cycles: one for the 16-bit multiply and another for the product to be added to the accumulated result. The multiplier produces a 31-bit signed word, which is held in two 16-bit registers (it multiplies the 2's-complement of two 16-bit data words). The result is 30 bits of data and 1 sign bit, which is left justified with a 0 LSB. The 16-bit accumulators require two passes for a 31-bit accumulate. The 16-bit-wide adder circuit has two 16-bit accumulators; you can keep two 16-bit running sums or a 32-bit sum that takes two passes through the adder. The multiplier is registered; each input is loaded into a register before passing through the unit's Booth multiplier. The resulting products are also registered. The ALU has two accumulators; an input from one accumulator can shift on its way to the ALU.

The μPD77C25 has a 24-bit instruction word and a 16-bit data word. The wider instruction word increases CPU execution efficiency. All instructions fit into a single instruction word, even instructions that carry immediate values. This scheme simplifies instruction-decode logic and ensures that all instructions (except branches) deliver apparent single-cycle execution. The instruction ROM has an 11-bit program counter, which automatically increments each cycle unless there is a branch, subroutine call, or interrupt. Hardware automatically saves the PC into a four-level LIFO hardware stack for interrupts and subroutine calls. If the CPU attempts more than four levels, the bottom value (first value stored) will be lost.

**Addressing modes**—Simple register-direct addressing. Two registers, DP and RP, hold the data RAM and ROM addresses. The complex instruction word defines an automatic increment/decrement for the DP and an automatic decrement for the RP pointers. Only 4 bits of the DP can be automatically adjusted to create a modulo-16 addressing loop. The register pointers can be loaded from the data bus and then automatically adjusted for each MAC cycle.

**Special instructions**—8-bit exchange, 1's-complement the accumulator (no divide instruction). The μPD77C25 lacks bit-manipulation instructions and hardware looping.

### VARIATIONS.

**μPD77C25**—8 MHz; 50 mA max at 5V; 2k×24-bit program ROM/EPROM/OTP; 512-byte data RAM; 28-pin DIP, 32-pin SOP, 44-pin PLCC. $8.70 to $12.90 (10,000).

## SUPPORT

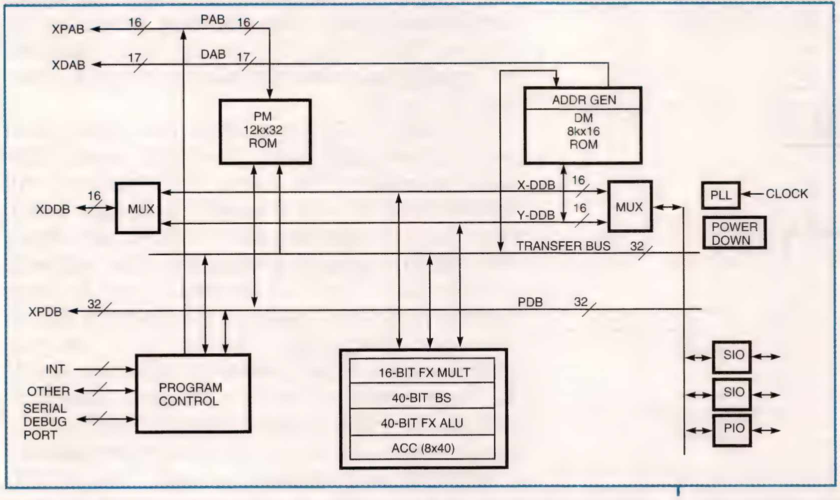
**HARDWARE.** An evaluation board, the EVAKIT-77C25, is available from NEC. It can also function as a limited ICE by plugging directly into the target-system DSP socket. The evaluation board with an adapter also plugs into standard PROM burners to program versions with EPROM or OTP memory.

**SOFTWARE.** No C compiler is available for the 77C20. NEC supplies an assembler-linker-loader package, and a third-party simulator is also available.

# NEC μPD77017
# 16-BIT FIXED-POINT DSP

## ARCHITECTURE

NEC's μPD77017 targets 16-bit digital-cellular, voice, and fax-modem applications. The 16-bit fixed-point μPD77017 combines a number of architectural features to ensure fast, single-cycle MAC execution. These features include three internal buses for X and Y data and transfer buses; a MAC unit; a barrel shifter; and eight general-purpose 40-bit register/accumulators. The DSP delivers apparent single-cycle (pipelined) instruction execution. The MAC unit is pipelined, too, and takes one cycle.



The μPD77017 has 16-bit data words and 32-bit instruction words. It has dual external memory ports—one for 16-bit data and one for 32-bit programs—with two distinct 16k-word address spaces for data. The 32-bit instruction word helps to minimize instruction-decoding logic and to increase code efficiency. Memory read/write accesses can take a single cycle, although instruction pipelining may require an extra cycle for some instructions. An on-chip wait-state generator lets the processor run with slower, less expensive memory. The 77017 supports both programmed and externally requested wait states. Like many of NEC's DSPs, the 77017 has an 8-bit host I/O port, which enables a host μP to exchange data with the DSP.

The 77017 neatly partitions into two major processor sections and a peripheral set. Main sections include the data unit and the program unit. The data unit contains X and Y memory units, each of which has an address generator, register file, and MAC-execution unit. The program unit contains the instruction-address unit with built-in loop control, interrupt-control logic, program memory, and instruction-decode/control logic. A transfer bus links the two main units. Each main unit connects to an external data-memory interface: 14-bit addresses and data for the data unit.

The data unit's MAC has three 40-bit parallel subunits: a multiplier, an ALU, and a barrel shifter. The MAC unit provides eight guard bits, but, because the 77017 does not support automatic saturation, results must be program manipulated to retain accuracy. Unlike many DSP implementations, the MAC subunits do not have dedicated input and output registers. Instead, the MAC is tightly integrated with a set of eight general-purpose registers. The X, Y, and transfer buses push data into the general register set; the general register set provides the data to drive the individual MAC subunits, which can execute concurrently. In effect, the general register set, which is basically a multiport register file, serves as the interchange that links the data side of the processor to the execution side.

Two 2-word ROM data-memory banks supply the X and Y data components for each MAC cycle. Each bank has its own address generator with a set of four address-pointer registers. Each unit also has an index-register link to the main data bus. Through this bus, code can load and modify the pointer and modification registers. Each unit also has a modulo register for modulo index addressing. A special bit-reverse circuit handles bit-reversed addressing for each bank.

On the program side, the DSP has a 12k-word (32-bit) instruction ROM and 256-word instruction RAM. The RAM must be loaded directly under program control. Additionally, the DSP hardware supports automatic looping with a four-level loop stack that lets code nest so it can loop under hardware control.

**Addressing modes**—Memory direct, register indirect, immediate. Hardware supports modulo and bit-reversed addressing for each data memory.

**Special instructions**—Conditional operations (minimize jumps), 1-bit shift-multiply-add, clip result, register-indirect subroutine call, register-indirect jump, single and block instruction hardware loop, repeat. The 77017 lacks bit-manipulation instructions. The DSP has a 15-level hardware PC stack that pushes the PC for interrupts and subroutine calls.

**VARIATIONS.**

**μPD77017**—33 MHz; 170 mA max at 3.3V; 12k×32-bit program ROM; 256×32-bit program RAM; 8k×16-bit data ROM; 4k×16-bit data RAM; 100-pin TQFP. $32 (10,000).

## SUPPORT

**HARDWARE.** NEC supplies a PC-based plug-in development board that offers in-circuit emulation using the 77017's on-chip emulation features. The board plugs into the PC/AT bus and links to the target board via a six-pin connector that connects to the 77017's on-chip ICE logic.

**SOFTWARE.** No C compiler is available for the 77C20. NEC supplies an assembler-linker-loader package, and a third-party simulator is also available.

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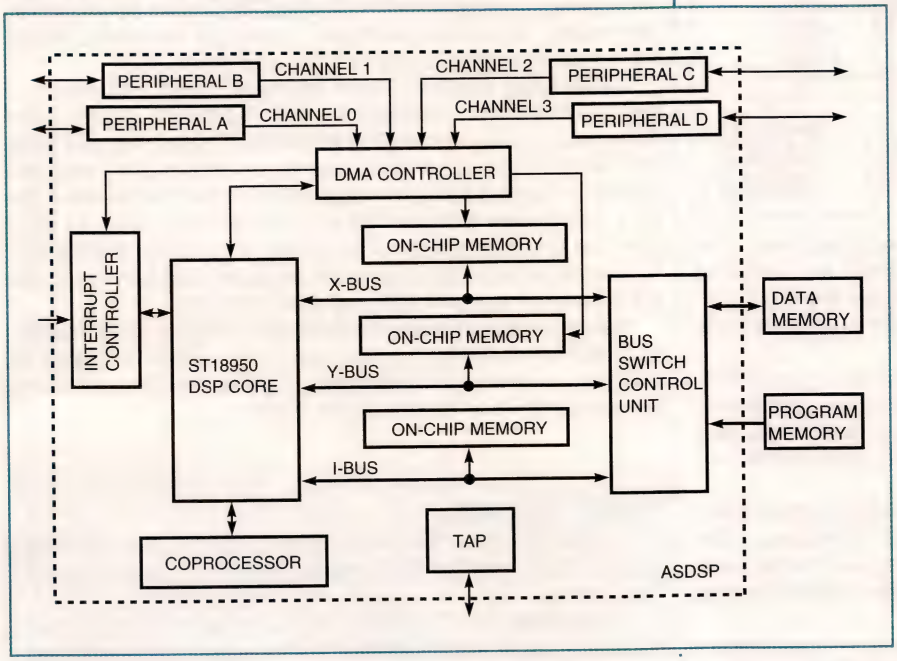
# SGS-THOMSON D950-CORE
# 16-BIT FIXED-POINT DSP CORE

## ARCHITECTURE

With its triple-level metal CMOS technology, the D950-Core can be embedded as a megafunction in a gate array or cell-based device that has a 0.5-μm library containing RAM, ROM, and PLAs. By simply adding optional peripherals such as an INT controller, DMA controller, bus-switch control unit, etc, as well as memory for data and instruction, you can customize a powerful application-specific digital-signal processor (ASDSP) around the D950-Core. The key to the D950-Core's performance is its high degree of parallelism, which allows the D950-Core to simultaneously perform multicycle functions along with other processors.



The D950-Core's architecture comprises a data-calculation unit (DCU), address-calculation unit (ACU), program-control unit (PCU), and an emulation-and-test unit (ETU). These units are organized around three bidirectional 16-bit buses—two for data and one for instruction. Each bus is dedicated to a unidirectional 16-bit address bus. Data memory (up to 128k words of RAM and ROM) and registers map on to the external data buses. Access to program RAM and ROM (up to 64k words) is via the instruction bus; data and instruction buses share the same bus-control interface.

Depending on the calculation mode, the D950-Core DCU computes operands, which can be 16- or 32-bit, signed or unsigned. The chip includes a 16×16-bit parallel multiplier to implement MAC-based functions (one cycle per MAC). A 40-bit arithmetic-and-logic unit (ALU) implements a range of functions with two 40-bit accumulators. The D950-Core has a 40-bit barrel-shifter unit and a bit-manipulation unit that handles MCU (master-controller-unit) processing through bit operations. Both 16/32-bit fractional (signed/unsigned) and 16/32-bit integer (signed/unsigned) word formats are available.

The D950-Core ACU generates an address for each of the two identical data memories and updates them at each instruction, allowing instruction execution and two register-to-memory moves in one cycle.

The D950-Core PCU updates the program counter (PC) according to the current instruction and/or internal and external events. It performs program-address generation, instruction fetch and decoding, exception processing, and hardware loop control. By default, the PC increments by 1.

The chip's ETU contains three independent parts that share the same external interface: an emulation port, core-scan registers (CSR), and a test port (for production-test purposes). Access to these units is via dedicated I/O pins, which allow the ETU to interface with an outside JTAG TAP controller or function as primary access to the final ASDSP chip, according to the IEEE 1149.1 JTAG standard.

An 8-bit general-purpose parallel port (P0 to P7) can be configured as an input or output. A test condition is attached to each bit to test external events; chip control is via interface pins related to interrupt, low-power mode, reset, and miscellaneous functions.

**Addressing modes**—direct, indirect-linear, indirect-modulo, indirect-bit-reverse (all with postincrement), indirect-indexed, and immediate.

**Special instructions**—bit manipulation, support double-precision calculations, support specific coprocessor instructions for integrated coprocessor.

## SUPPORT

**HARDWARE.** SGS-Thomson offers a JTAG PC board with a graphic windowed high-level source debugger for ASDSP emulation.

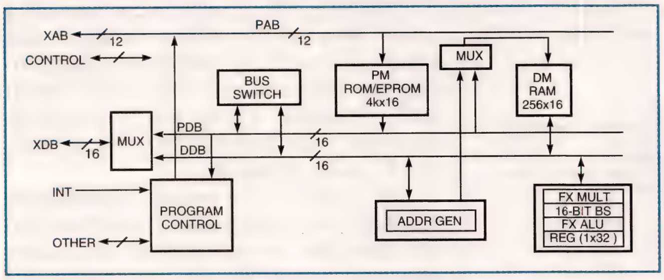
**SOFTWARE.** A C compiler, simulator, and assembler/linker that run on PC/Sun systems are available, as well as a Synopsys VHDL model.

# TEXAS INSTRUMENTS TMS320C1X FAMILY 16-BIT FIXED-POINT DSP

## ARCHITECTURE

TI's TMS320C1x has a large collection of application code supporting a large range of applications. The chip requires careful assembly-language programming, but costs have dropped to the point that C1xs are competitive with many µPs and µCs. In volume, C10s cost less than $3 apiece.

This DSP family is accumulator-based; however, the accumulator is 32 bits wide for double-precision, 2's-complement arithmetic. Although the accumulator lacks guard bits, the DSP has an automatic saturation mode for rounding. The architecture relies on shared resources, such as buses and memories, rather than implementing multiple sets to speed processing. The modified Harvard architecture separates program and data accesses, yet allows transfers between code and data spaces to share resources.



A MAC operation takes two cycles and two instructions, first the multiply and then the add instruction. Addressing for the MAC data values is not automatic; a basic MAC pass requires code to specifically address, fetch, and operate on each set of X, Y data values.

The TMS320C10 has a single data bus, limiting data reads or writes to one per cycle. For each MAC operation, code must load the multiplier's T register with one data value then move the second data value to the multiplier before starting the multiply.

The MAC's 16-bit barrel shifter, in parallel with the single-cycle, 16-bit multiplier, feeds into a 32-bit ALU that handles both 16- and 32-bit operations. The accumulator feeds back to the ALU. The accumulator then feeds a simple shifter (shifts 0, 1, or 4 bits over) that, in turn, links to the data bus.

A logic section that has its own program bus and memory handles code fetch and decoding. This section has a 4-deep hardware stack (8 on the C16) that holds PC values for interrupts or subroutine branches. Data in the program ROM or EPROM can transfer to the data RAM and then be used as constants for MAC series expansion.

**Parallel I/O ports**—You can use the 16-bit external data bus as an I/O port to connect external peripherals such as ADCs or DACs. Separate I/O select signals let you use up to eight separate I/O ports on the bus (16 with the C14).

**Event manager**—The C14 event manager adds a capture-and-compare subsystem to supplement the C14's two 16-bit timer/counters. The subsystem has six 16-bit compare and six 16-bit capture registers. Compare-register values are compared with the running timers; on a match, the subsystem generates an interrupt or an external signal. A high-precision PWM mode adds 2 bits of additional resolution for PWM outputs (resolution is 40 nsec at 25.6 MHz). The subsystem can capture events; changes in one of six input lines trigger logic to set the timer/counter value in a capture register. The subsystem has a FIFO stack that can buffer up to four capture values for four capture registers.

**Companding hardware**—On the C17, this hardware "compands" (compresses and expands) data for serial or parallel mode. It handles both the A- and µ-Law forms, which meet American, Japanese, or European standards.

**Addressing modes**—Paged memory direct addressing: 7 bits in instruction concatenate with 9-bit data-page pointer for accessing data RAM (128 words each page); register indirect addressing (uses 8 bits from one of the auxiliary registers to address data RAM); and immediate. Most members of the C1x family have a limited off-chip addressing range (12 bits); the C16 is the exception with 16-bit addressing. Additionally, the external addressing is for program memory only; the C1x does not support off-chip data memory.

**Special instructions**—No hardware looping or bit manipulation, instruction to move value one position higher in memory, transfer data between program and data memory, test input pin and branch if pin is zero.

### VARIATIONS.

**TMS320C10**—25.6 MHz, 94 mA max at 5V; 288-byte RAM; 3-kbyte ROM; 16-bit parallel I/O port; 44-pin PLCC. $4 (1000).

**TMS320C14**—25.6 MHz, 50 mA max at 5V; 512-byte RAM; 8-kbyte ROM/EPROM; 16-bit parallel I/O port; two timers; 16-bit watchdog timer; one baud-rate-generation timer; 68-pin PLCC. $8 (1000).

**TMS320C15**—25.6 MHz, 85 mA max at 5V (16 MHz, 50 mA max at 3.3V); 512-byte RAM; 8-kbyte ROM/EPROM; 40-pin DIP; 44-pin ceramic leaded chip carrier; 44-pin PLCC. $5.60 (1000). AT&T Microelectronics also sells an ASIC macro for this device.

**TMS320C16**—35 MHz, 100 mA max at 5V (25.6 MHz, 65 mA max at 3.3V); 512-byte RAM; 16-kbyte ROM; 64-pin PQFP. $6.06 (1000).

**TMS320C17**—20 MHz, 65 mA max at 5V (14.4 MHz, 22.7 mA max at 3.3V); 512-byte RAM; 8-kbyte ROM/EPROM/OTP; two serial I/O ports; one timer; 8/16-bit asynchronous coprocessor port; 40-pin DIP; 44-pin PLCC. $5.06 (10,000).

## SUPPORT

**HARDWARE.** An ICE and evaluation modules (PC add-in card) are available from TI. Many third-party vendors sell hardware development tools for the C1x.

**SOFTWARE.** TI furnishes a development tool kit with an assembler/linker, simulator, and application library. Many third-party tools are also available.

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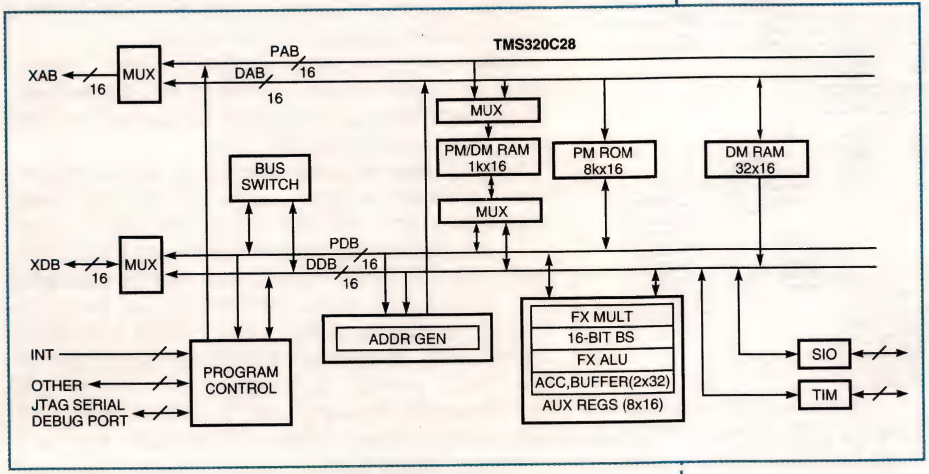
# TEXAS INSTRUMENTS TMS320C2X FAMILY 16-BIT FIXED-POINT DSP

## ARCHITECTURE

The TMS320C2x is TI's second-generation 16-bit, fixed-point DSP family. Source-code-compatible with the first-generation C1x, C2x processors still rely on a multiplier-accumulator combination. However, TI designers supplemented those resources with a parallel 32-bit ALU, including a carry bit (although there are still no guard bits) and eight auxiliary registers. Similar to the C1x, the C2x supports automatic saturation rounding. The C2x improved on the C1x's limitations. External memory addressing is 16 bits (64k words each for data and code), and it has 24 new instructions, including a repeat instruction (with automatic data-address increments for MAC operations) as well as expanded on-chip RAM to include two 512-byte data blocks for X and Y memories supplemented by 64 bytes of RAM. Program ROM is 8 kbytes, and DMA simplifies external access to internal memory. All versions have a synchronous serial port and a timer.



The TMS320C2x runs a basic MAC cycle in two cycles—one to multiply and one to accumulate. The MAC instruction handles a multiply on current variables and an accumulate using the last cycle's accumulated value. The chip can access two on-chip data (or program) RAMs in a single cycle to feed the multiply for a MAC cycle. However, unlike later DSPs, C2x code must explicitly handle data addressing for the next MAC cycle, unless the MAC instruction is a repeated instruction. In that case, the data and program/data block addresses increment automatically.

The C2x has a modified Harvard architecture and maintains two separate memory and bus systems, one each for data and program code. In certain applications, the single data bus limits data reads or writes to one per cycle. On-chip program accesses do not interfere with DSP data manipulation. Code and data share a common external memory bus; each has its own 64k-word address space with a pin differentiating between the data and program address spaces. With a fast enough external memory, a C2x delivers single-cycle (pipelined) instruction execution by accessing instructions or one of the data values from external memory. However, you can use slower memory to cut costs; the C2x hardware generates memory wait states (using a Ready pin) to stretch out access times. The C2x has support to access up to 16 I/O ports through its external data bus.

With the C2x, you don't have to write code loops to repeat key instructions. TI added a repeat-instruction capability, with which you can repeat an instruction up to 255 times. Also, the eight-level hardware stack automatically extends into memory, thus enabling code to deal with deep subroutine and interrupt nesting.

**Addressing modes**—Paged-memory direct addressing: 7 bits in instruction concatenate with 9-bit data-page pointer for accessing data RAM (128 words each page); register indirect addressing (uses 16 bits from one of the auxiliary registers to address data RAM); and immediate. Software can use the auxiliary registers to hold indirect pointers as well as to index the address. Indirect address registers can be postincremented/decremented to minimize addressing overhead. Indirect-addressing options include bit-reversal addressing.

**External DMA**—External devices can take control of the C2x's internal buses and read or write on-chip memories. When the HOLDA signal pulls down, the C2x processor halts, opening memory to external access.

**Special instructions**—Load T (multiply) register and accumulate previous product; load T register, accumulate previous product, and move data; multiply and accumulate; multiply and accumulate previous product; square and accumulate; square and subtract previous product; call subroutine indirect; block move (used with repeat instruction, program to data, data-to-data memory); table R/W; test bit (in memory); hardware looping to repeat single instruction.

### VARIATIONS.

**TMS320C25**—50 MHz, 185 mA max at 5V; 1088-byte RAM; 8-kbyte ROM/EPROM; 68-pin PLCC. $11.60 (1000). AT&T Microelectronics also sells a macro for this device.

**TMS320C26**—50 MHz, 220 mA max at 5V; three 1-kbyte data/program RAM blocks; 64-byte data RAM; 512-byte boot ROM; multiprocessor support; 68-pin PLCC. $10.50 (1000).

## SUPPORT

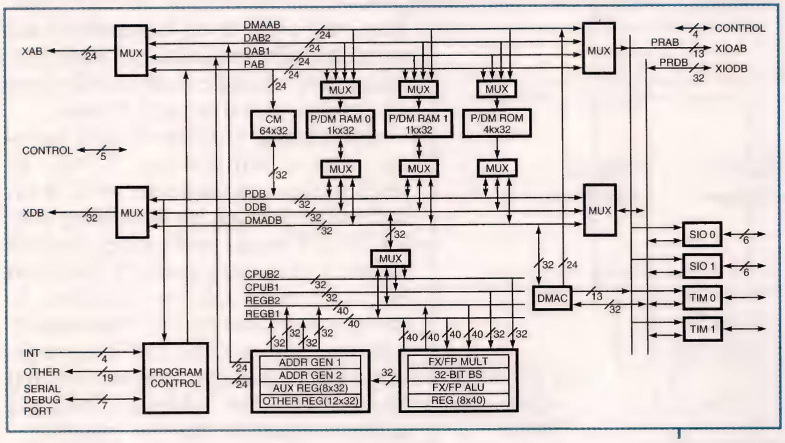
**HARDWARE.** TI provides a software development board and evaluation boards that use built-in emulation logic in the C2x. Third-party tools are also available. Contact TI.

**SOFTWARE.** TI supplies a C compiler, source-level debugger, assembler/linker, simulator, and application library. Third-party tools are also available. Contact TI.

# TEXAS INSTRUMENTS
# TMS320C3X FAMILY
# 32-BIT FLOATING-POINT DSP

## ARCHITECTURE

TI's third-generation DSP, the TMS320C3x, is a 32-bit processor that integrates a Von Neumann μP architecture with a high-performance, 32-bit, floating-point DSP MAC core. On the microprocessor side, the C3x supports a unified, flexible, 24-bit address space (16 Mbytes×32). On the DSP side, the C3x processor performs single-cycle MAC processing. The processor receives the next instruction while accessing two data values for the current instruction's MAC cycle. The C3x family does not support IEEE floating-point formats.



Three subsystems make up the TMS320C3x DSP: memory/access, central core, and I/O subsystems. The memory/access subsystem comprises separate program, data, and DMA buses, which allow parallel program fetches, data reads and writes, and DMA operations. This internal busing scheme enables programs to access the next instruction and two data values simultaneously as well as transfer data to or from the I/O subsystem in one cycle. The data address buses share a single data bus that can make two sequential RAM accesses in a single cycle. Two 32-word, lockable, on-chip caches automatically load as instructions are accessed from external memory. The two 4-kbyte RAM blocks hold parameters and constants for sum-of-products MAC processing, and a large ROM can hold code or coefficients for MAC processing.

A minisystem in its own right, the central core has its own set of buses to move data and results; these buses move data between internal registers, an integer/floating-point multiplier, a parallel 32-bit barrel shifter/ALU, and the memory subsystem. Results are stored in extended-precision or auxiliary registers that hold the values. Two address generators in the subsystem generate the addresses to access the memory/access subsystem's data memories. The major core registers, eight 40-bit extended-precision registers, auxiliary registers, and key-control registers, are held in a central multiported register file.

The third C3x subsystem, the I/O subsystem, comprises a single-channel DMA controller (dual channel in C32) and a collection of peripherals interlinked with the peripheral address and data bus set. The DMA controller uses the memory/access subsystem's DMA bus to access on-chip memory. The memory/access subsystem buses pass through a multiplexer and link to the peripheral bus, which serves the DMA controller and peripherals. On the C30, the peripheral bus links to an external expansion bus with a 13-bit address bus and 32-bit data bus.

**Addressing modes**—Register direct, paged-memory direct, register indirect, and immediate; circular addressing to support circular buffers; and bit-reversed addressing for FFTs.

**Special instructions**—Single or block instruction hardware looping (supports nestable block repeats but lacks automatic save and restore of status), standard/delayed branches (standard empties pipe; delayed waits three cycles before changing PC), interlocked access instructions for multiprocessing (load/store integer or FP value and signal interlocked), computed GOTOs (dynamic subroutine calls), convert floating-point to integer and vice versa. Bit manipulation is limited to bit test. You can specify instructions to execute in parallel. The hardware has a memory-based stack.

### VARIATIONS. (priced at 10,000 units)

**TMS320C30**—33 to 50 MHz; 600 mA max at 5V (excludes 50-MHz version); 4k×32-bit program ROM; 2k×32-bit data RAM; two timers; two serial ports; expansion bus. In 181-pin PGA, 33-MHz version, $135; 40-MHz version, $156. In 208-pin PQFP, 40-MHz version, $66; 50-MHz version, $75.

**TMS320C31**—33 to 60 MHz; 325 to 475 mA max at 5V; 2k×32-bit data RAM; boot ROM; two timers; serial port. In 132-pin PQFP, $38 to $50.

**TMS320LC31**—33/40 MHz; 300 mA max at 3.3V (excludes 40-MHz version); 2k×32-bit data RAM; boot ROM; two timers; serial port. In 132-pin PQFP, $42 to $46.

**TMS320C32**—40 to 60 MHz; 390 to 475 mA max at 5V; 512×32-bit data RAM; boot ROM; two timers; serial port; two low-power modes; flexible system-memory interface (8, 16, or 32 bits wide). In 144-pin PQFP, $24 to $31 (in quantities of 250,000, this device sells for <$10).

## SUPPORT

**HARDWARE.** TI supplies a full-speed ICE and an evaluation module. Third-party vendors have hardware tools for the C3x. Contact TI for references. HP has an ICE for the C30/C31. The C3x lacks JTAG support but, instead, has a proprietary five-pin emulation interface.

**SOFTWARE.** TI sells a tool set that includes a C and C++ compiler, assembler/linker, source-level debugger, code profiler, simulator, and application library. Third-party tools include C and Ada compilers, an OS (Spox), filter-design packages, and advanced graphical-design tools.

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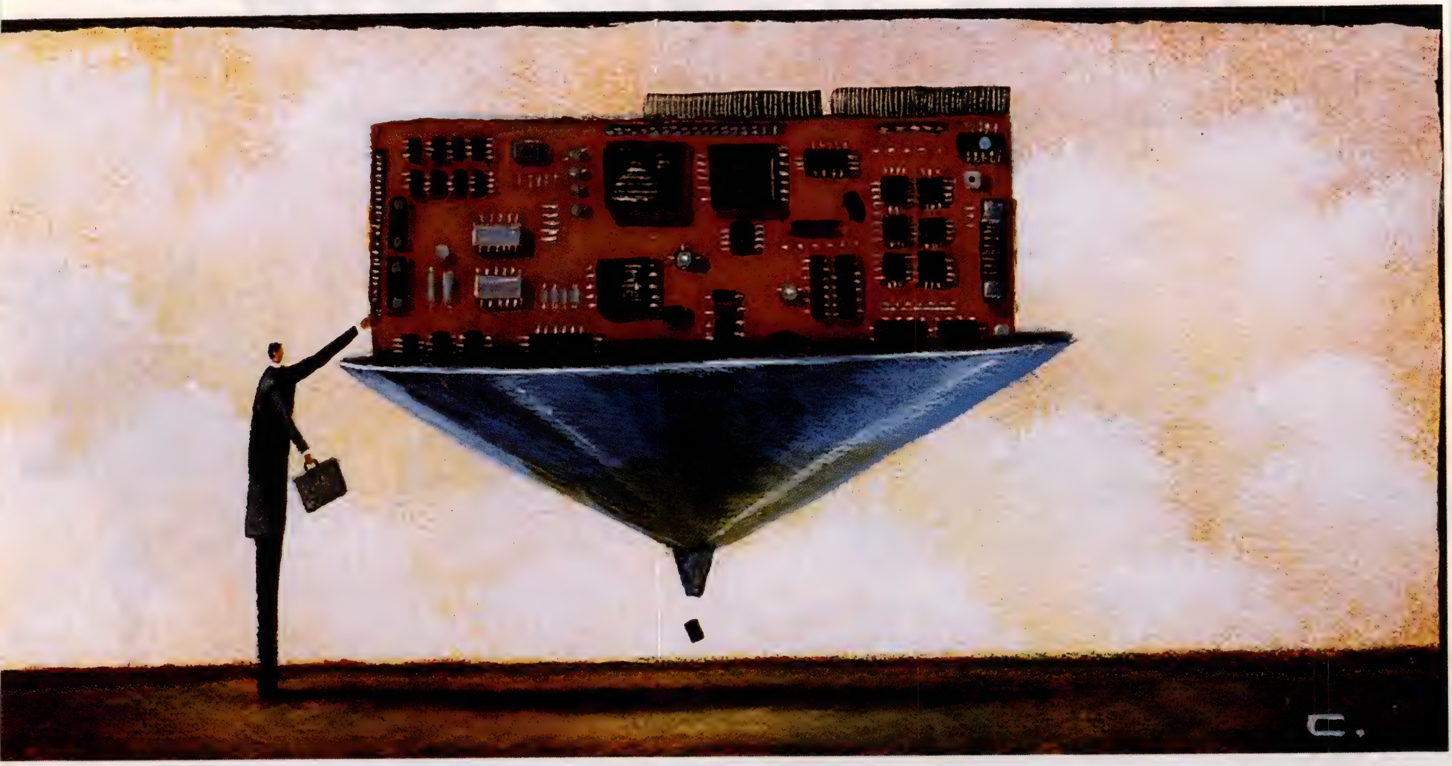

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| CS5509 | 16 | 1 | 20/200 |

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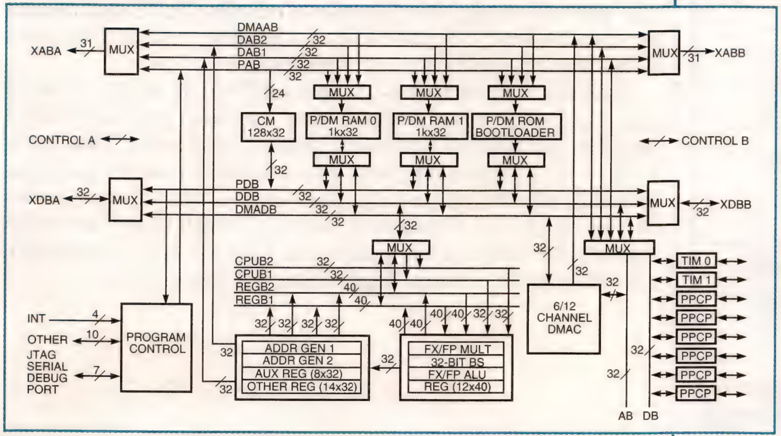
# TEXAS INSTRUMENTS
# TMS320C4X FAMILY
# 32-BIT FLOATING-POINT DSP

## ARCHITECTURE

The C4x is more than just a fast, floating-point DSP chip: It provides a new level of parallel processing. TI engineers added six independent communications ports for point-to-point links to other C4x processors. The ports are backed with a sophisticated DMA subsystem that has its own internal buses. The C4x is popular for multiprocessor applications and is making a dent in the multiprocessing market previously dominated by the SGS-Thomson Transputer, which has point-to-point serial communications links.



As a DSP engine, the C4x has seven internal buses and on-chip memories that help deliver single-cycle execution while walking through X, Y memories for a series of MAC operations. A 128-word cache enables the processor to deliver single-cycle pipelined execution and still use slower external memory (the cache is not used with internal memory). Key inner routines fill the cache as they run. When the CPU accesses an instruction from external memory, it automatically loads the instruction into cache, which is divided into four 32-word segments or lines. The CPU uses an LRU algorithm to select the cache segment for the new instructions. You can freeze a segment in the cache by setting cache-freeze bits in the CPU status register.

The C4x is built around a five-port register file, and, rather than time-sharing a single bus system, it features separate buses for program and two data fetches. Additionally, the C4x has three separate functional units: the FPU multiplier, ALU, and barrel shifter for parallel operations.

TI engineers equipped the C4x with six 8-bit independent communications ports for point-to-point communications with networks of C4xs and peripherals (the C44 only has four ports). Each port consists of eight data pins and four handshake signals. These ports free the 31-bit local and global external memory buses for program or data accesses to the processor's 4G-word address space (C40 only). Program and data occupy a unified address space that you can configure according to your memory requirements. The local and global buses have different memory-block assignments within each memory space. I/O can also use the external buses.

A sophisticated six-channel DMA subsystem with its own address and data buses moves data between the communication ports and memory without altering the CPU's sequential threads. Such data movements do not load down the DSP processor with servicing overhead, although some data contention for memory may slow CPU execution.

**Addressing modes**—Register direct, paged-memory direct, register indirect, and immediate. Circular addressing to support single-size circular buffers. The CPU applies bit-reversed operations to register indirect addressing only.

**Special instructions**—Single or block instruction zero-overhead hardware looping (supports nestable block repeats but lacks automatic save and restore of status), standard/delayed branches, interlocked access instructions for multiprocessing (load/store integer or FP value and signal interlocked), convert floating-point to integer and vice versa, reciprocal and reciprocal square root seed, conversion to and from IEEE floating-point formats. Bit manipulation is limited to bit test. You can specify certain instructions to execute in parallel. The hardware has a memory-based stack.

### VARIATIONS.

**TMS32C40**—40/50/60 MHz; 680/850/1020 mA max at 5V; 4k×32-bit boot ROM; 2k×32-bit data RAM; two timers; 325-pin PGA. $160/$178/$196 (10,000).

**TMS32C44**—50/60 MHz; 850/1020 mA max at 5V; 4k×32-bit boot ROM; 2k×32-bit data RAM; two timers; 24-bit external address buses; power-down mode; 304-pin PQFP. $99/$110 (10,000).

## SUPPORT

**HARDWARE.** Development system includes scan-based emulation via the C4x's JTAG test port. External hardware can use the JTAG port to control the processor as well as to set and to monitor registers or memory. You can also string multiple C4x chips on a JTAG circuit for parallel debugging. One processor breakpoint can halt execution in an array of C4x chips, and you can single-step them all in lock step. TI sells a C4x evaluation board (with four processors) that works with a number of host platforms. Third-party tools are also available. Contact TI for a vendor list.

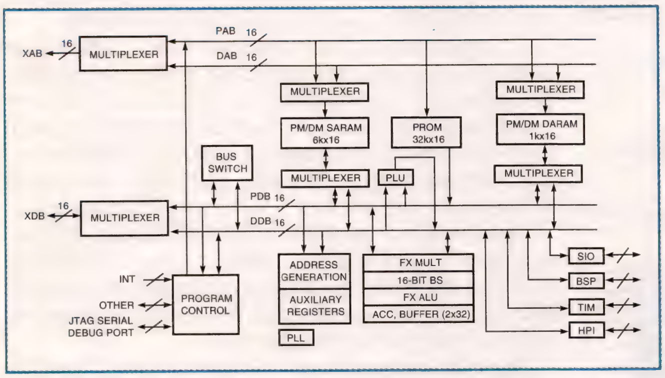
**SOFTWARE.** Tools include a C compiler, Ada and C++ compilers, source-level debugger for parallel debugging, assembler/linker, and simulator. TI also has an application library. Third-party support includes the Spox, Parallel C, Virtuoso, and Helios operating systems.

# TEXAS INSTRUMENTS TMS320C5X FAMILY 16-BIT FIXED-POINT DSP

## ARCHITECTURE

The TMS320C5x, source-code-compatible with the C2x, is TI's highest performance 16-bit fixed-point DSP family. A static CMOS design, the C5x runs at up to 100 MHz (20-nsec instruction cycle).

The TMS320C52 DSP CPU is offered as an application-specific-processor (ASP) core for a TI gate array, the TEC320C52. It combines 10k usable gates for special logic, 8k words of ROM, and 2k words of RAM. The gate array runs at 57.1 or 80 MHz.



The TMS320C5x is both an accumulator-based and a register-based processor. It has a fixed MAC circuit with a registered, 16×16-bit multiplier loading a 32-bit product register. The product register, in turn, feeds a 32-bit accumulator (no guard bits). The C5x also has two parallel functional units feeding off the data bus: an independent ALU with a register file of eight auxiliary registers and a bit-logic processing unit. Multiply and accumulate take one cycle each. The basic MAC cycle involves putting a value into a temporary register, fetching a second value, multiplying into a holder register, and accumulating the result in the next cycle. However, if the MAC instruction is executed within a hardware loop, the DSP can achieve single-cycle execution.

For embedded applications, TI engineers added fast context switching and bit-level operations. To minimize the overhead for saving the CPU state or context on an interrupt, the C5x has a 1-deep shadow register stack for the major registers (accumulator, accumulator buffer, product and status registers, three temporary registers, index register, and auxiliary compare register). The C5x also has an eight-level hardware stack for storing the program counter. For control applications that need bit manipulation, TI engineers added a parallel logic unit (PLU) that runs in parallel with the MAC and ALU circuits. The PLU operations can set, clear, test, or toggle multiple bits in a control/status register or data-memory location. The C5x also has 0- to 16-bit left and right data barrel shifters.

**Power-down mode**—Minimizes power by shutting down the CPU (IDLE1 instr) or the CPU and the peripherals (IDLE2). Pulling down an external pin (HOLD*) can also force the chip into power-down mode. An interrupt brings the chip up to normal run conditions.

**Addressing modes**—Paged memory direct addressing: 7 bits in instruction concatenate with 9-bit data-page pointer for accessing data RAM (128 words each page), indirect, immediate, dedicated register, memory-mapped register. The processor supports automatic circular buffer addressing for two buffers; however, this addressing mechanism lacks wrap-around capability on overshoot.

**Special instructions**—Single and block repeat, load T (multiply) register and accumulate previous product; load T register, accumulate previous product, and move data; multiply and accumulate; multiply and accumulate previous product; square and accumulate; square and subtract previous product; call subroutine indirect; block move (use with repeat instruction and program to data, data-to-data memory); table R/W; test and manipulate bit in memory.

### VARIATIONS.

**TMS320C50**—40/57/80 MHz; 60/67/94-mA max at 5V (core portion only); 20-kbyte program/data RAM; 4-kbyte ROM; two serial ports; one timer; 132-pin PQFP. $32/$42/$48.

**TMS320C51**—40/57/80 MHz; 60/67/94-mA max at 5V (core portion only); 4-kbyte program/data RAM; 16-kbyte ROM; two serial ports; one timer; 132-pin PQFP/100-pin TQFP. $21/$23/$25.

**TMS320C52**—40/57/80 MHz; 60/67/94-mA max at 5V (core portion only); 2-kbyte program/data RAM; 8-kbyte ROM; one serial port; one timer; 100-pin PQFP/TQFP. $13/$14/$17.

**TMS320C53**—40/57/80 MHz; 60/67/94-mA max at 5V (core portion only); 8-kbyte program/data RAM; 32-kbyte ROM; two serial ports; one timer; 132-pin PQFP/100-pin TQFP. $31/$34/$39.

**TMS320LC56/LC57/C57S**—57/80 MHz; 36/53-mA max at 3.3V (core only); 14-kbyte program/data RAM; 64-kbyte ROM (57S has 4-kbyte ROM); two buffered serial ports; one timer; one host port interface (LC57 and C57S only); 100-pin TQFP (LC56)/128-pin TQFP (LC57 and C57S). $41 to $54.

## SUPPORT

**HARDWARE.** The C5x is TI's first fixed-point DSP with a JTAG serial scan port for chip test and ICE-like debug control and monitoring. TI supplies a DSP starter kit, an evaluation module, and an emulator based on the C5x's built-in emulation logic. Third-party tools are also available.

**SOFTWARE.** TI supplies a C compiler, source-level C assembler/debugger, assembler/linker, simulator, profiler, and application library. Third-party tools are also available.

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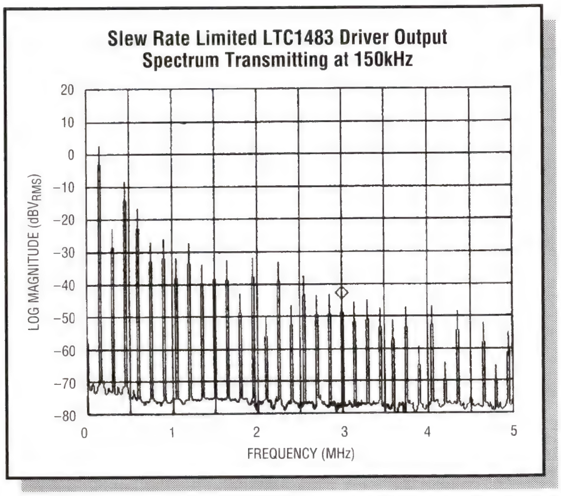

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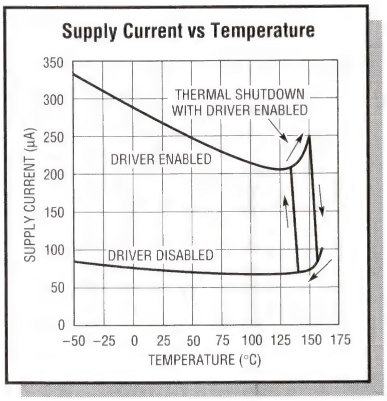

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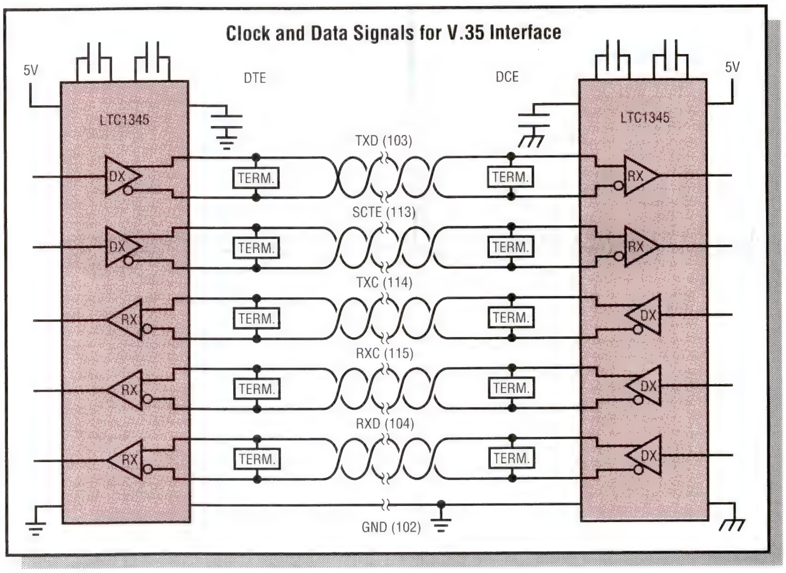

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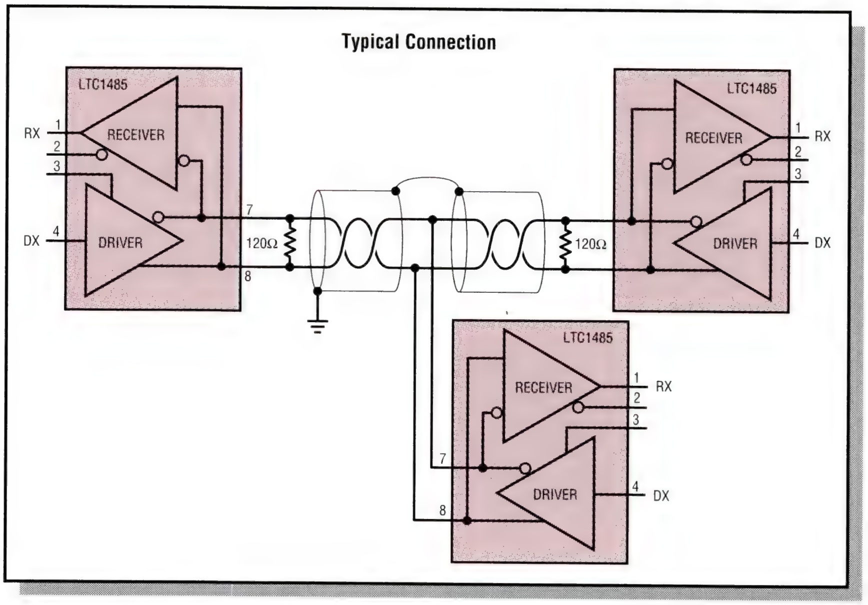
Typical Connection

The low power LTC1485 transceiver draws only 1.8mA from its single 5V supply, but guarantees data rates to 10Mbits/s. System reliability is enhanced with the best overvoltage performance in the industry and thermal shutdown to protect against bus contention.

Other features include:

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- Supports RS485 and RS422
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This device is the choice for high speed data transfer in industrial controls and instrumentation, and commercial network systems. Available in 8-lead DIP and SOIC, pricing starts at only $1.64 in thousands.

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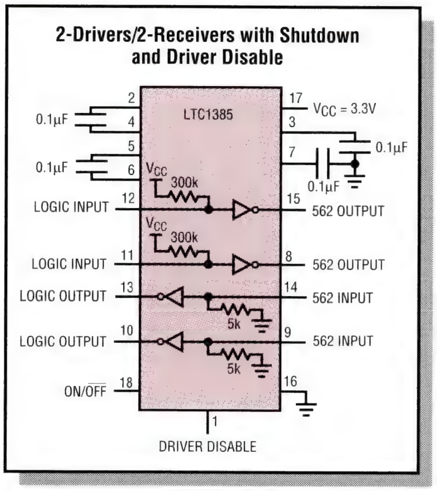
# Ultra-Low Power, Single Supply RS232 and EIA562 Transceivers for 3.3V Systems


2-Drivers/2-Receivers with Shutdown and Driver Disable

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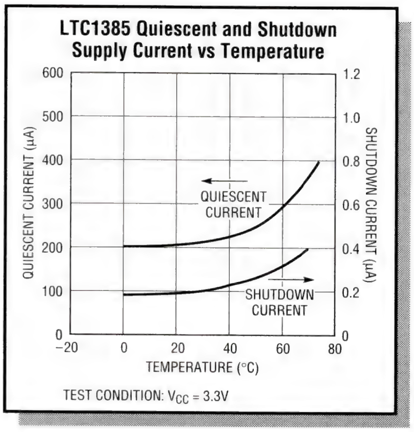
LTC1385 Quiescent and Shutdown Supply Current vs Temperature

TEST CONDITION: $V_{CC}$ = 3.3V

For 2-driver/2-receiver applications including hand-held 3.3V systems such as inventory checkers and palmtop computers, use the ultra-low power of the LTC1385 EIA562 transceiver with its 200µA supply current and shutdown. DIP, SOL, and SSOP are available with pricing beginning at $3.30 in thousands.

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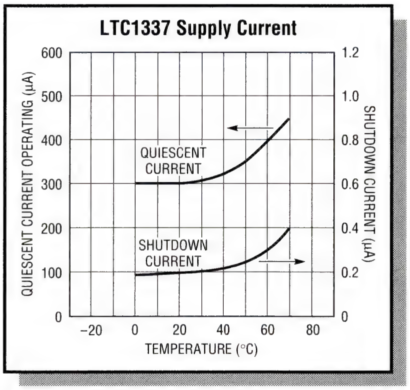
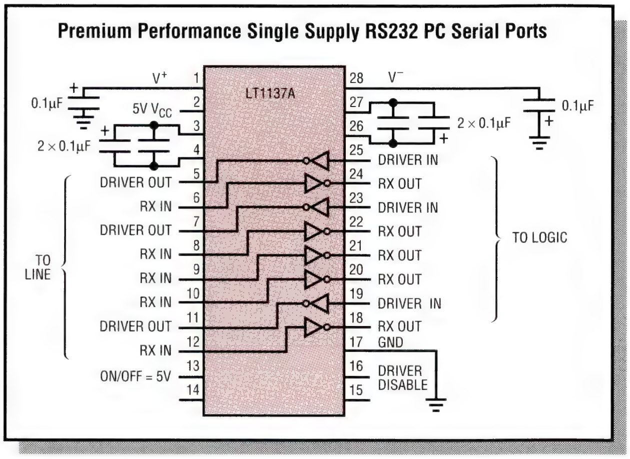

**LTC1337 Supply Current**


**Premium Performance Single Supply RS232 PC Serial Ports**

The ultra-low power CMOS compliment to the LT1137A is our LTC1337. It features a supply current slashed to 300µA and a 1µA Shutdown mode. The LTC1337 supports data rates above 120kbaud, has plenty of output to drive a mouse, and offers rugged ESD protection. Ideal for battery-powered PC serial ports, the LTC1337 is available in DIP, SOL, and SSOP, priced from $4.53 in thousands.

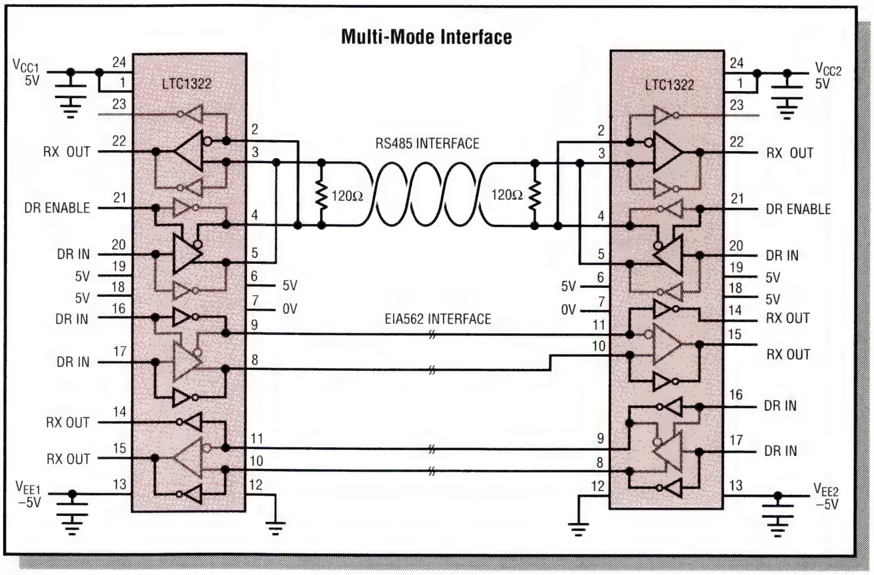
Circle No. 218: Please send literature.    Circle No. 219: Call me. I'm interested.

# Combined Mode 232/562/485 Transceivers for Programmable Interface Ports

The LTC1321 and LTC1322 are versatile, multi-protocol interface transceivers for proprietary or programmable interface ports. Key features include pin-programmable configuration, loopback for diagnostic testing, and a power-saving Shutdown mode.

- LTC1321 driver/receiver pairs: one RS232/562, one RS485
- LTC1322 driver/receiver pairs: two RS232/562, two RS485
- Low supply current: 1mA typical
- 15µA supply current in Shutdown
- Drivers go high impedance in three-state, Shutdown, or with power off

With prices starting at only $4.49 (LTC1321, 1000pc. quantities), these are excellent choices for programmable I/O ports, mainframe computers, digital multiplexers, and networks.


**Multi-Mode Interface**

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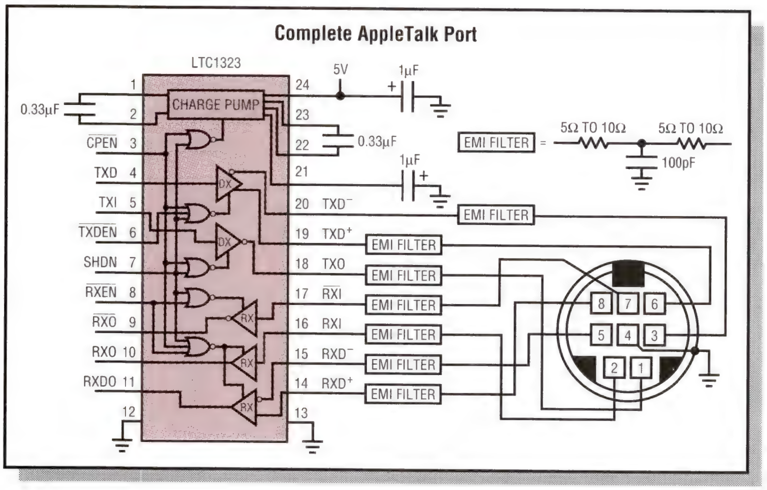
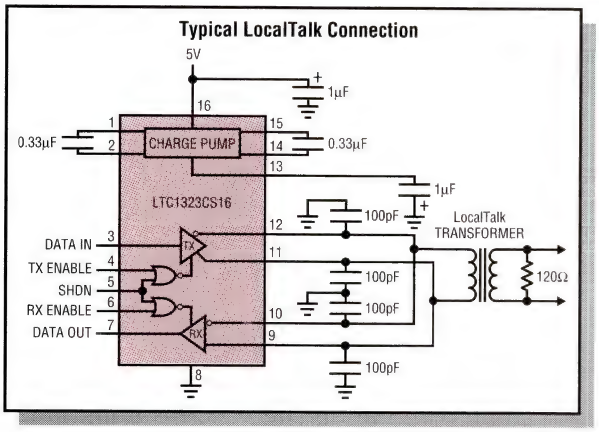
# Complete AppleTalk®/LocalTalk® Transceivers Run from Single 5V Supplies

The LTC1323 and the LTC1323-16 are rugged single supply transceivers that provide complete AppleTalk (LTC1323) or LocalTalk (LTC1323-16) ports for computer networks. Receiver inputs and driver outputs are ESD protected with proprietary clamping cells. Low power operation (2.4mA typ) and a 0.5μA Shutdown mode make this an ideal choice for battery-powered systems. Average power use for the LTC1323 can be further reduced with a micropower receiver that stays active to receive data, while the rest of the device lies idle.


Complete AppleTalk Port


Typical LocalTalk Connection

Available in SOL, SSOP, and narrow SOIC (LTC1323-16) packages, these devices are excellent solutions for LocalTalk peripherals, desktop, notebook, or PDA computers with AppleTalk networking. 1000-piece pricing starts at $4.70 for the LTC1323 and at only $4.30 for the LTC1323-16.

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| ISOLATION VOLTAGE | INPUT CURRENT | MAX INPUT FREQUENCY | GLITCH-FREE OUTPUT FILTER | EXT CLOCK SYNCH | UL RECOGNIZED | PART NUMBER |
|---|---|---|---|---|---|---|
| 2500$V_{RMS}$ | 700μA | 200kHz | Yes | Yes | ЯU | LTC1145A |
| 2500$V_{RMS}$ | 70μA | 20kHz | Yes | Yes | ЯU | LTC1146A |

| ISOLATION VOLTAGE | INPUT CURRENT | TIME ON/ TIME OFF | DRIVES ANY LOGIC LEVEL FET | CURRENT LIMITED | UL RECOGNIZED | PART NUMBER |
|---|---|---|---|---|---|---|
| 2500$V_{RMS}$ | 2.5mA | 2.5ms/1ms | Yes | Yes | ЯU | LTC1177 |

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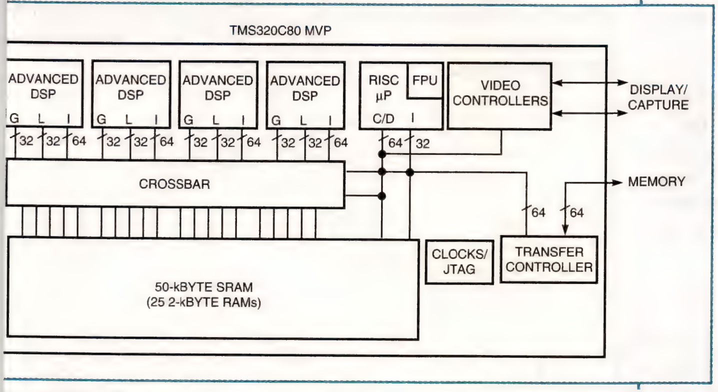
# TEXAS INSTRUMENTS TMS320C80 32-BIT MULTIPROCESSOR DSP

## ARCHITECTURE

TI's 4-million-transistor TMS320C80 (previously known he Multimedia Video Processor or MVP) integrates four allel-processing DSPs (PPDSPs) and a 32-bit RISC master cessor (MP) on a single chip. The 'C80 processes multiple ks in parallel (each assigned to a specific processor), col- tively delivering 2-BOPS (billion-operations/sec) perfor- nce. The 'C80's processing suits a range of real-time appli- ions, such as video compression/decompression, communications, image recognition, and audio.



The 'C80's five processors execute independently and con- rently. A high-speed, on-chip crossbar connects the CPUs h 25 2-kbyte blocks of dedicated SRAM, which provides he and RAM for each CPU. Any processor can access any 16 SRAM blocks, although five blocks are dedicated to each U. The crossbar handles up to 15 simultaneous RAM esses/clock cycle: three per PPDSP, two for the MP, and e for the transfer controller (TC). Peak crossbar bandwidth .2 Gbytes/sec. Memory-mapped control registers handle h transfer and video controllers (VCs); the chip has a sep- te 32-bit data path between the MP, TC, and VC, which bles the MP to set register values.

The 'C80 has high processor throughput: Each CPU exe- es from its own crossbar-memory instruction cache—2 tes for the PPDSPs and 4 kbytes for the MP. The MP also 4 kbytes of crossbar-memory data cache. Executing from ssbar instruction caches, the CPUs achieve apparent sin- -cycle execution.

The PPDSPs have a 64-bit instruction word with three jor subfields for controlling the data unit (with a 32-bit U and 16-bit multiplier) and each of two independent lress units. Each address unit has a 32-bit data path to the crossbar and can also be used for general-purpose math. Three zero-overhead loop controllers support nested looping. The 32-bit ALU can split into two 16-bit ALUs or four 8-bit ALUs; the multiplier performs one 16×16 multiply or two 8×8 multiplies. Additional hardware supports bit-field and pixel processing.

The MP has an integrated 64-bit floating-point unit (FPU) that shares a common 31×32-bit register file with integer processing. A register scoreboard flags registers that are waiting on loads from memory or from the FPU to keep operations in order without unnecessary waiting.

The MP's FPU incorporates a single-precision FP multiplier and a double-precision FP adder. It also supports vector processing with built-in vector operations and four accumulators to hold interim vector results. Both the MP's main integer path and its FPU units are pipelined. The MP has a three-stage pipeline. A single-precision multiply or double-precision addition normally take four cycles to complete but are pipelined, so they can finish every cycle. The integer unit triggers FPU operations, which proceed independently. Vector instructions can start a multiply, add, and load or store every cycle, yielding a peak performance of 100 Mflops.

The 'C80 is more than just a collection of CPUs and memory; it has its own on-chip I/O and memory controller, the TC, which provides an adaptive memory interface with automatic byte alignment, as well as both linear and X, Y (frame buffer) addressing. It supports SDRAM, DRAM, VRAM, and SRAM and also has a video controller to minimize design for video applications. The VC supports two video frames (all video timing signals). It also has a special serial-register-transfer (SRT) controller for controlling VRAM frame memories by the TC.

**Addressing modes**—Indexed, base, immediate, relative.

**Special instructions**—Bit and byte manipulation, log base 2, many types of compare instructions. It supports neither conditional execution nor hardware looping for single and block repeat and has no hardware stack.

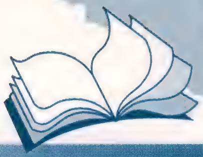
### VARIATIONS.

**TMS320C80**—50 MHz; 3300 mA max at 3.3V; 305-pin CPGA. $400 (10,000).

## SUPPORT

**ARDWARE.** The 'C80 supports multiple processor akpoints: one CPU can breakpoint and halt execution of CPUs on the chip. TI sells a parallel-processing ICE )S510) that handles debugging of multiple 'C80 chips. ughborough Sound Images Ltd (Loughborough, Leicester- re, UK, phone 1509-634300) and Precision Digital Images dmond, WA, (206) 882-0218) sell hardware-development tems. The 'C80 supports JTAG.

**SOFTWARE.** TI sells a tool set that includes an assembler/linker, C compiler, simulator, and parallel debugger. The debugger includes the MP Debugger and multiple PPDSP debuggers. Parallel Debug Manager handles and coordinates individual CPU debuggers. TI fields a multitasking executive that runs on the MP, interfaces to a host CPU, and issues commands to 'C80's PPDSPs. Spectron Microsystems' (Santa Barbara, CA) Spox real-time, multitasking operating system ($12,000) has been ported to the 'C80.



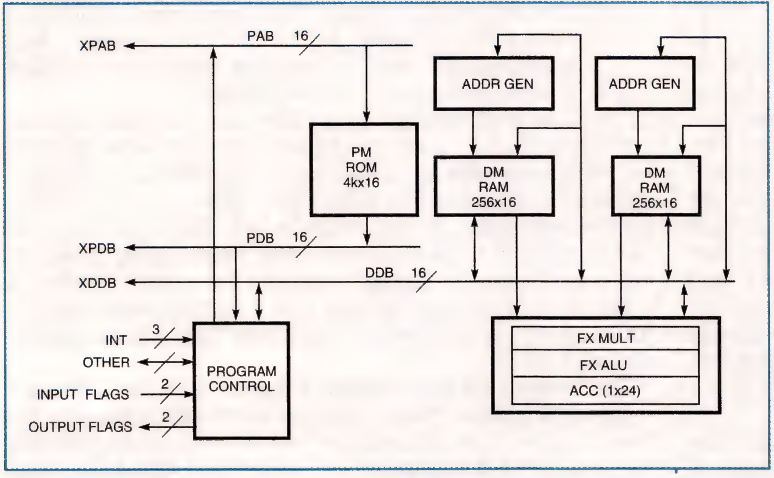
# ZILOG Z893XX FAMILY 16-BIT FIXED-POINT DSP

## ARCHITECTURE

Zilog added DSP chips and DSP-enhanced µCs to its line to handle math-intensive processing applications. An on-chip codec interface makes the Z89321 well suited for voice, audio, and digital-cellular applications.

The Z893x40 has a compact, accumulator-based DSP architecture built around a single-cycle MAC unit, which includes a 16×16- to 24-bit multiplier, 24-bit product register, and 24-bit accumulator and ALU (no guard bits). The DSP processor runs from a 4k-word program ROM/OTP (the Z89391 can also access 64k words of external program memory). Two internal bus sets—a program address/data bus set and a data address/data set—prevent program thread execution from interfering with cycle-by-cycle MAC processing.

Two RAM blocks hold program coefficients and data, which feed directly into the MAC's input registers each cycle. Results land in a product register and 24-bit accumulator each cycle. RAM block addressing automatically increments or decrements the address, which eliminates the need for data-address-generation code for each MAC cycle.



The basic DSP chip has two external buses: an external program bus (Z89391 only) and an I/O bus. External data must come in on the I/O bus. An external-memory R/W takes one cycle. A single wait state may be inserted using software control; the WAIT pin can be used for additional wait states. Running code from external memory takes one additional cycle for each instruction—the data is read in one cycle but is not available for processing until the next instruction cycle.

The CODEC interface is compatible with 8-bit PCM and 16-bit CODECs. Many general-purpose 8- and 16-bit ADCs and DACs are adaptable. The interface can also be used as a high-speed serial port. Z893xx chips also have two 13-bit timers: one dedicated to the CODEC interface and the other to general purpose.

**Addressing modes**—Memory direct (to 512 RAM wor register indirect (to RAM or ROM with pointer registe immediate, short-form direct (uses 16-bit data register RAM), external peripheral addressing (one cycle, tr peripheral as a register). Modulo addressing options incl modulo 2 to 256 processing loops.

**Special instructions**—Compare register to accumula conditional execution of certain instructions as well as c ditional branching and subroutine calls. The Z893xx c not perform repeat (hardware looping) or bit manipulati For subroutines and interrupts, the Z893x1 has a six-l hardware stack.

### VARIATIONS.

**Z89321**—20 MHz; 60 mA max at 5V; 512-word RAM 4k-word mask ROM; 40-pin DIP; 44-pin PLCC/QFP. $3.7 (10,000).

**Z89371**—16 MHz; 60 mA max at 5V; 512-word RAM 4k-word OTP ROM; 40-pin DIP; 44-pin PLCC/QFP. $7.4 (10,000).

**Z89391**—20 MHz; 60 mA max at 5V; 512-word RAM ROMless; 16-bit external instruction bus; 84-pin PLCC $5.66 (10,000).

## SUPPORT

**HARDWARE.** Zilog sells an evaluation board and ICE for the Z893xx, as well as for the combined Z8/Z89 chips. The Z893xx does not support JTAG.

**SOFTWARE.** Zilog fields a C compiler, assembler/linl simulator, source-level debugger, and application librarie also has a TMS320-to-Z893xx assembly-code translator.

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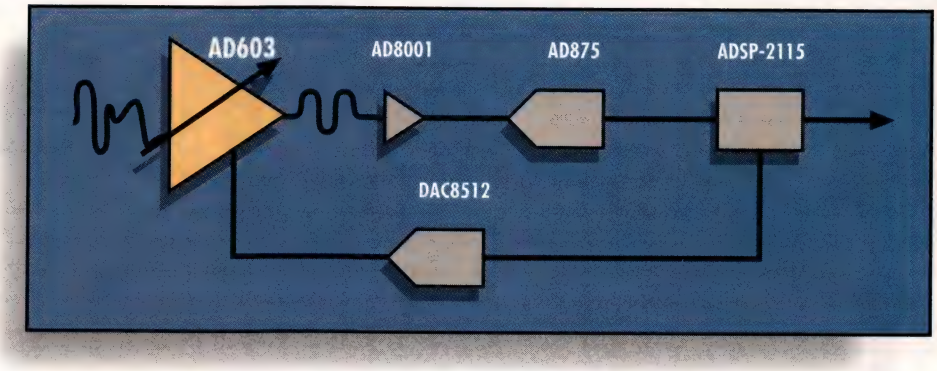

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| Input Noise Spectral Density | 1.4 nV/√Hz | 1.4 nV/√Hz | 1.3 nV/√Hz |
| Signal Gain Accuracy (typ) | ±0.25 dB | ± 0.25 dB | ±0.4 dB |
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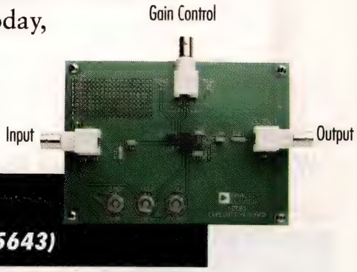

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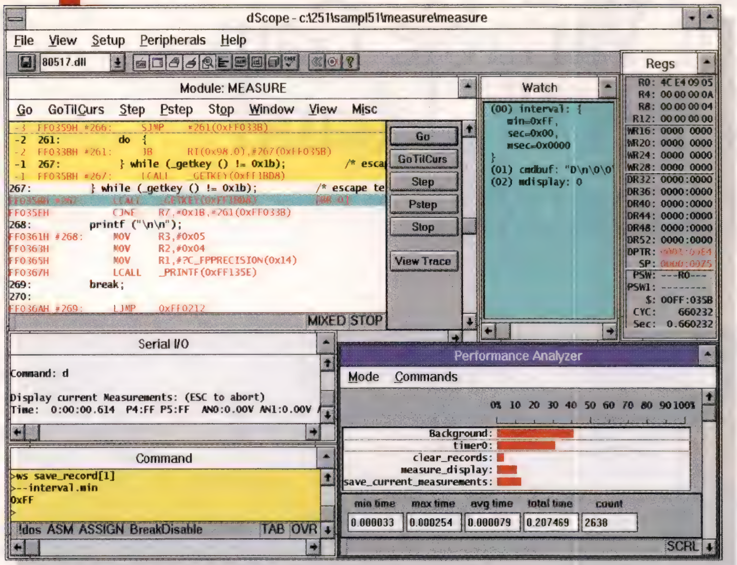
CIRCLE NO. 11

# THE 8051 & 251 DEVELOPMENT TOOL EXPERTS

KEIL SOFTWARE™



```
-3  FF0359H #266:     SJMP    #261(0xFF033B)
-2  261:          do  {
-2  FF033BH #261:     JB      RI(0x98.0),#267(0xFF035B)
-1  267:          } while (_getkey () != 0x1b);          /* escaı
-1  FF035BH #267:     LCALL   _GETKEY(0xFF1BD8)
267:          } while (_getkey () != 0x1b);          /* escape te
FF035BH #267:     LCALL   _GETKEY(0xFF1BDA)          [RB 0]
FF035EH           CJNE    R7,#0x1B,#261(0xFF033B)
268:          printf ("\n\n");
FF0361H #268:     MOV     R3,#0x05
FF0363H           MOV     R2,#0x04
FF0365H           MOV     R1,#?C_FPPRECISION(0x14)
FF0367H           LCALL   _PRINTF(0xFF135E)
269:          break;
270:
FF036AH #269:     LJMP    0xFF0212
```

```
(00) interval: {
   min=0xFF,
   sec=0x00,
   msec=0x0000
}
(01) cmdbuf: "D\n\0\0
(02) mdisplay: 0
```

```
  R0: 4C E4 09 05
  R4: 00 00 00 0A
  R8: 00 00 00 04
 R12: 00 00 00 00
WR16: 0000  0000
WR20: 0000  0000
WR24: 0000  0000
WR28: 0000  0000
DR32: 0000:0000
DR36: 0000:0000
DR40: 0000:0000
DR44: 0000:0000
DR48: 0000:0000
DR52: 0000:0000
DPTR: 0001:00E4
  SP: 0000:0075
 PSW: ---R0---
PSW1: --------
   $: 00FF:035B
 CYC:     660232
 Sec:   0.660232
```

```
Command: d

Display current Measurements: (ESC to abort)
Time:   0:00:00.614  P4:FF P5:FF   AN0:0.00V AN1:0.00V
```

```
>ws save_record[1]
>--interval.min
0xFF
>
```

```
               Background:
                   timer0:
            clear_records:
          measure_display:
save_current_measurements:

min time   max time   avg time   total time   count
0.000033   0.000254   0.000079   0.207469     2638
```

*dScope-251: Windows™ based 8051 & 251 debugger*

# C51

# Version 5

## *The best 8051 C compiler just got better...*

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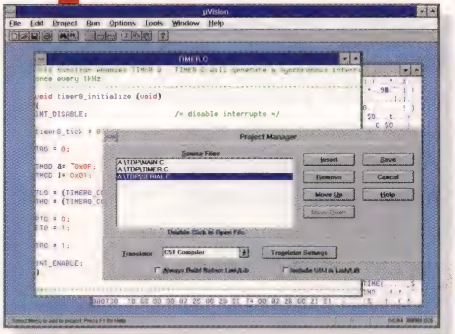
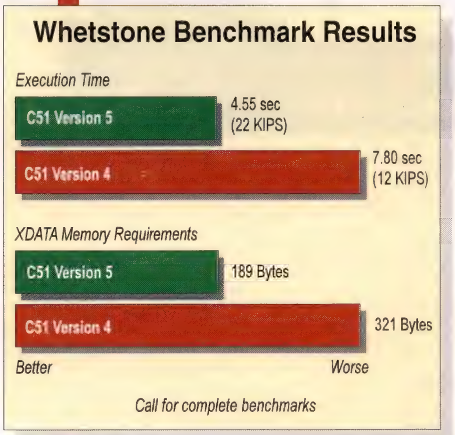
To better support our customers in the United States and Canada, **Keil Software, Inc.** has opened a new sales and support office in Dallas, Texas. Previously, the Keil 8051 development tools were marketed under the Franklin brand name. Now, customers can get upgrades and technical support directly from Keil Software.



*µVision/251 Windows™ IDE*



*C51 Benchmark Comparison*

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Phone: ++49 89 / 46 50 57
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**US Distributors:** Franklin, Nohau, MetaLink, Hitex, Emulation Technology

**International Distributors:** **Australia**: Electro Optics 02/654 1873 **A**: Rekirsch 01/2597 2700 **B**: Bytecom 010/223 455 **Czech Rep**: ComAp 2/684 8862 **CH**: Redacom 032/410 111, Thau 01/740 4105 **DK**: Nohau 043/446 010 **E**: CAPEL 93/217 2340 **F**: Convergie 1/4904 9200 **I**: BRM 011/437 1551, NORD 02/6610 4160 **IRL**: Ashling 061/33 44 66 **Israel**: ITEC 03/491 202 **NL**: Tritec 01858/16133 **PL**: WG 022/217 704 **S**: Nohau 040/922 425 **Singapore**: Testtech 65/7492162 **SLO**: ASYST 061/445526 **South Africa**: Eagle (021) 23 4943 **Taiwan**: Demmax 35/772772 **Turkey**: EMPA 1/599 3050 **UK**: Hitex 01203/692 066, Nohau 01962/733140

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**CIRCLE NO. 67**

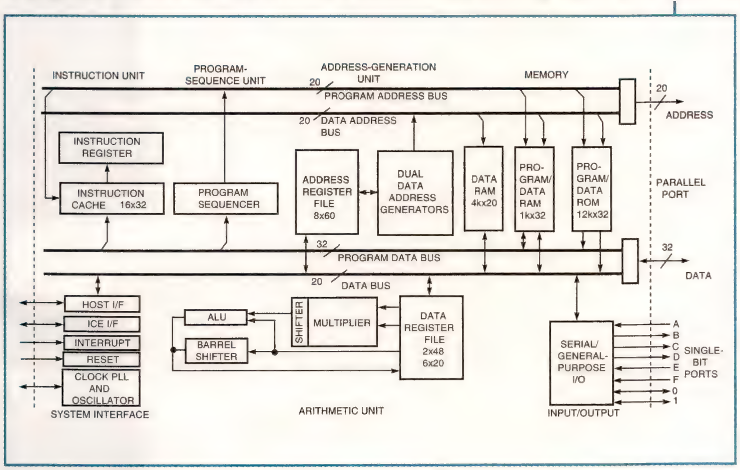
# ZORAN ZR38001
# 20-BIT FIXED-POINT DSP

## ARCHITECTURE

Zoran's ZR38001 was developed for a specific application class in tandem with Dolby Laboratories. The ZR38001 delivers a 0.67-msec 1024-point complex FFT and a 132-nsec Radix-2 FFT Butterfly.

The ZR38001 is a load/store-register-oriented architecture that lends itself to straightforward coding. To minimize decoding and instruction overhead, Zoran relies on a 32-bit instruction word; however, the ZR38001 has a 20-bit data word to minimize cost.

The ZR38001 has an on-chip instruction cache that holds the last 16 instruction words executed. Running from the cache, the three-stage-pipeline CPU can start an instruction every cycle. The hardware uses a delayed-branch instruction that will execute the next two instructions before it takes a branch.



The ZR38001 architecture supports multiple operations per instruction cycle. For MAC class cycles, it can generate two data addresses per cycle, as well as fetch the next instruction. For dual data addressing, the chip has two data address generators and has an 8×60-bit address register file. Using a basic 66-MHz internal clock (external 33 MHz), the hardware can access its on-chip RAM twice during a single 33-nsec cycle. Thus, the processor can make do with a single data RAM, even for dual-access MAC operations. The hardware supports FFT bit reversal and modulo addressing for DSP processing. It incorporates zero-overhead looping, with up to four stacked loops.

An address register file (ARF) expands addressing capabilities: It incorporates a 20-bit stack pointer and eight address sets. The programmer must set up the stack pointer to an appropriate memory location; this procedure is in lieu of a hardware stack. Each address set consists of three 20-bit registers: address, index, and modulus. You can also use the ARF registers as general registers or for I/O.

Arithmetic operations center on a multiport register file, which handles up to three data reads, two writes, and two reads or writes per instruction cycle, enabling the hardware to read data for the next operation while returning results for the current operation. The register file has eight 20-bit registers. Two of the registers extend to 48 bits to support 48-bit accumulation (8-bit overflow). The hardware incorporates a 48-bit ALU and barrel shifter and a 20×20-bit multiplier.

The ZR38001 supports a 20-bit, 1M-word, unified program/data address space. The chip has a 20-bit external address bus and 32-bit external data bus. Internally, the chip builds on a dual bus system with a 20-bit data address bus and data bus set, and a 20-bit program address bus and 32-bit program data bus set. The hardware feeds the external address bus by multiplexing the internal program and data address buses. Similarly, the external data bus links through a bidirectional multiplexer to the 32-bit program data bus and 20-bit data bus. The ZR38001 supplies six serial I/O ports that suit multimedia applications.

**Addressing modes**—Register direct, memory direct, and register indirect addressing (all with increment/decrement), indexed, immediate, bit-reversed, or circular modulus options. For table walking, you can postincrement/decrement by 1 or by an index value.

**Special instructions**—Absolute Value, bit manipulation, FFT Butterfly Primitive (multiplies two registers and adds/subtracts a third register, stores sum, and divides), Compare, Compare Absolute, Delayed Branch (executes next two instructions before branch), Signed/Unsigned Divide Iteration (bit step), Move Max/Min (moves max/min value from array), Normalize (also for max mantissa). The ZR38001 also performs hardware looping for single and multiple instructions. The chip has no conditional execution or rotation instructions.

### VARIATIONS.

**ZR38001**—33 MHz; 500 mA max at 5V; 12k×32-bit program ROM; 1k×32-bit program RAM; 4k×20-bit data RAM; six half-duplex serial ports that can be used as a serial host interface; 128-pin PQFP. $42 (1000).

## SUPPORT

**HARDWARE.** Zoran sells a ZR38001 development board. PC/AT ISA bus-compatible, the board can be dropped into a standard PC/AT (and above). It has an interface to external analog systems. The ZR38001 has JTAG-compatible ICE support.

**SOFTWARE.** Zoran supplies software-development tools, which run on MS-Windows on x86-based PCs. The tools include an assembler/linker, simulator, and debugger. Zoran has the following software modules for the ZR38001: Dolby AC-3 six-channel surround decoding, Dolby AC-3 two-channel surround downmix decoding, MPEG-1 audio decoding/encoding, and Dolby Prologic decoding.

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CIRCLE NO. 186

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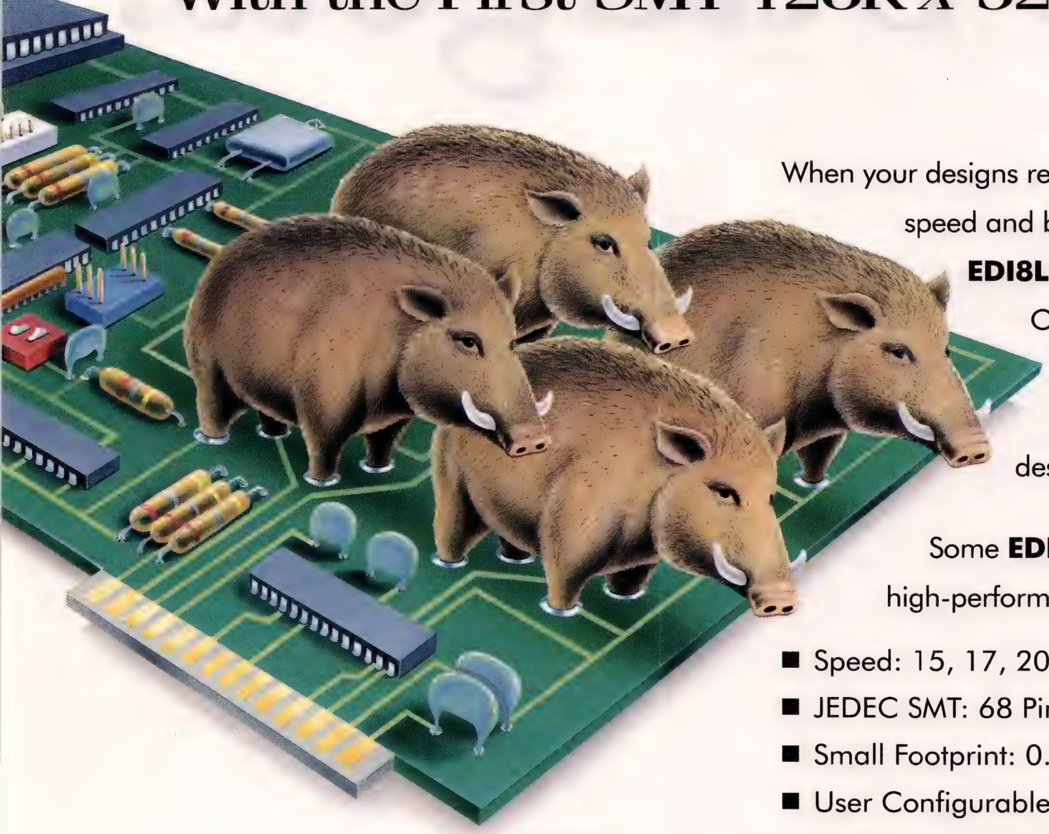

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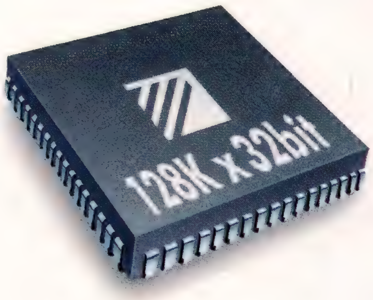

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CIRCLE NO. 215

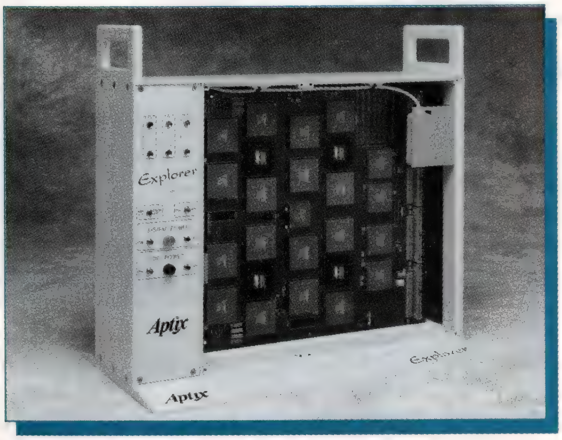
# DSP$^x$ '95 product preview

STEVEN H LEIBSON, EDITOR IN CHIEF

**This year's DSP$^x$ show, at the San Jose Convention Center, San Jose, CA, May 16 to 18, expands to encompass all forms of signal processing and associated EDA tools. The conference program features three technology tracks: DSP, Advanced analog and mixed signal, and ASIC and EDA. The DSP program addresses the changing world of DSP technology and its impact on product development across industries. The Advanced analog and mixed signal program features design techniques for the layout of mixed analog and digital boards that meet signal-integrity and performance requirements with high first-pass yields. The ASIC and EDA track explores DSPs as an integrated function to ASIC design techniques and methodologies that can be leveraged by complex EDA tools. Each track features general sessions, tutorials, case studies, technical seminars and keynote addresses.**

**For additional information, contact Reed Exhibition Co, Norwalk, CT, (203) 840-5652.**

**The following sample of products gives you a glimpse of the tremendous variety at the DSP$^x$ exhibits.**

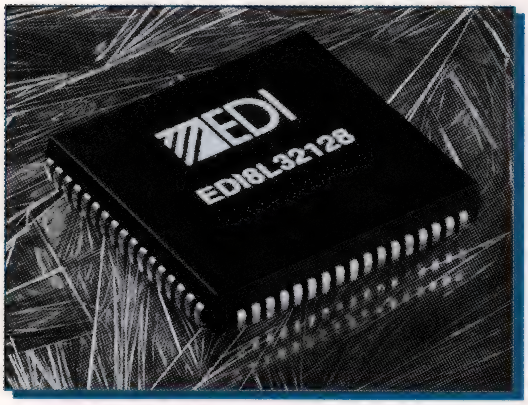


**ASIC-emulation system runs at 50 MHz.** Software and hardware enhancements allow the System Explorer line of ASIC-emulation boards to pattern IC designs at speeds to 50 MHz. The software automatically partitions logic from synthesized VHDL and Verilog designs into the multiple field-programmable gate ar-rays on the emulation board. After partitioning, the product's Automation Manager can perform place-and-route operations using a network of Unix workstations. This parallel-processing approach can cut design-iteration time to less than 1 hour/cycle. Complete hardware/software versions of the System Explorer start at $40,000. Hardware-only "replicas" each cost $12,760. **Aptix Corp, San Jose, CA.** (408) 428-6200. **Circle No. 456**

**Three-chip set builds 40-Mbps QAM transmission system.** The GC2011 digital filter chip, GC3011 resampler IC, and GC3021 carrier-removal chip comprise a three-chip set. The chip set is capable of receiving, equalizing, and demodulating quadrature amplitude modulation (QAM) signals at transmission rates to 40 Mbps. The chips cost $220, $143, and $107.60 (1000), respectively. You can use the GC2011 alone to build a QAM transmitter. **Graychip, Palo Alto, CA.** (415) 323-2955. **Circle No. 457**

**EDA tool targets multiprocessor DSP systems.** Virtuoso Synchro is a system-level electronic-design-automation (EDA) environment for specifying and designing synchronous, multirate DSP applications for multiprocessor target systems. The $16,700 product runs under

Microsoft Windows or Sun Solaris. Applications for the tool include speech and audio processing, radar, image and video processing, and telecommunications. The product has board-specific support for the TMS320C40 DSP $\mu$P, and code ports are in progress for other processors, including Analog Devices' 21020 and 21060, Texas Instruments' 320C80, and Motorola's 56000. **Eonic Systems Inc, Linden, Belgium. (32) 16-62 15 85.** **Circle No. 458**



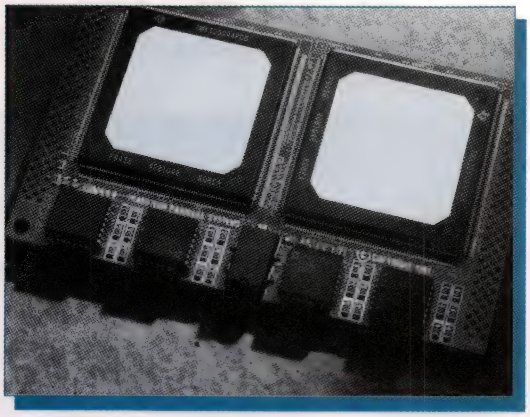
**Fast, wide SRAM modules suit DSP applications.** The vendor's SRAM modules suit the width and speed needs of DSPs. The latest device, the 128k×32-bit EDI8L 32128, is packaged in a PLCC. This memory is available in 17-, 20-, and 25-nsec versions. The 17-nsec version costs $234 (100). In addition, the company will soon announce 12- and 15-nsec versions. Other available memories include the 1M×8-bit EDI8F81025C ($335 (100) for a 70-nsec device, $614 (100) for a 35-nsec device); the EDI9F81025C-BPC, which is a dual 512k×8-bit device ($369 (100) for a 70-nsec device); and the 512k×32-bit EDI8F32512C, which is packaged in a 72-pin ZIP ($1386 (100) for a 35-nsec device). **Electronic Designs Inc, Westborough, MA. (508) 366-5151.** **Circle No. 459**

**JPEG compression software runs on the TMS320C3X.** This software package performs discrete cosine transforms, quantization, zigzag scanning, run-length encoding, and Hoffman coding per the Joint Photographic Experts Group (JPEG) standard for still-image compression and decompression. A source-code license costs $15,000, and an object-code license costs $9000. **MultiDSP, Lomita, CA. (310) 985-4899.** **Circle No. 460**

**ISA board carries two C31 floating-point DSPs.** The PC-C31 Aruba is a $2495 ISA bus PC-expansion card with two 40-MHz TMS320C31 floating-point DSPs, 2 Mbytes of zero-wait-state SRAM, and two high-speed RS-422 serial ports. The SRAM is split into asymmetric banks, one per DSP. One bank contains 1.5 Mbytes; the other contains 512 kbytes. In addition, each DSP can access a dual-ported, 8-kbyte RAM. Software-development support for either DOS or Windows includes a C compiler, an assembler, a linker, and an emulator. **Ariel Corp, Highland Park, NJ. (908) 249-2900.** **Circle No. 461**

**Numerical-analysis software runs on Power Macintosh computers.** HiQ is a $695 numerical-analysis software package for data acquisition, instrument control, numerical analysis, and data visualization. The software now runs on Apple's Power Macintosh computers, which have two to eight times more performance than high-end Quadra Macs. The package includes more than 600 math functions and a set of application-specific "problem solvers" and can generate 3-D graphs. The problem solvers can handle numerical integration, expression evaluation, optimization, ordinary differential equations, polynomial roots, nonlinear analysis, data fitting, integrals, and other complex mathematical problems. **National Instruments, Austin, TX. (512) 794-0100.** **Circle No. 462**

**Development systems for ADSP2105 DSP start at $159.** The E5 series of development systems for Analog Devices' ADSP210X DSPs comprises a development board, an assembler, example software, and utility routines, such as FFTs and DTMF encoding/decoding. The E5-1 includes the base processor, a boot ROM, and support circuitry on a 3.25-in.$^2$ pc board. The E5-2 adds 14 kbytes each of program and data RAM. The E5-3 adds a prototyping area, and the E5-4 adds two 16-bit, 44.1-kHz analog I/O channels using Analog Devices' AD1849 stereo codec. **The Athena Group, Gainesville, FL. (904) 371-2567.** **Circle No.463**



**VME card accepts two TIM-40 and two IndustryPak cards.** The $2650 TDMB424 is a VME carrier card with locations for two TIM-40 DSP modules and two IndustryPak I/O cards. The TDM44x series of TIM-40 cards carries one or two TMS320C44 DSPs and up to 4 Mbytes of SRAM or 12 Mbytes of DRAM. Prices for the TDM44x series start at $1495. **Transtech Parallel Systems, Ithaca, NY. (607) 257-6502.** **Circle No.464**

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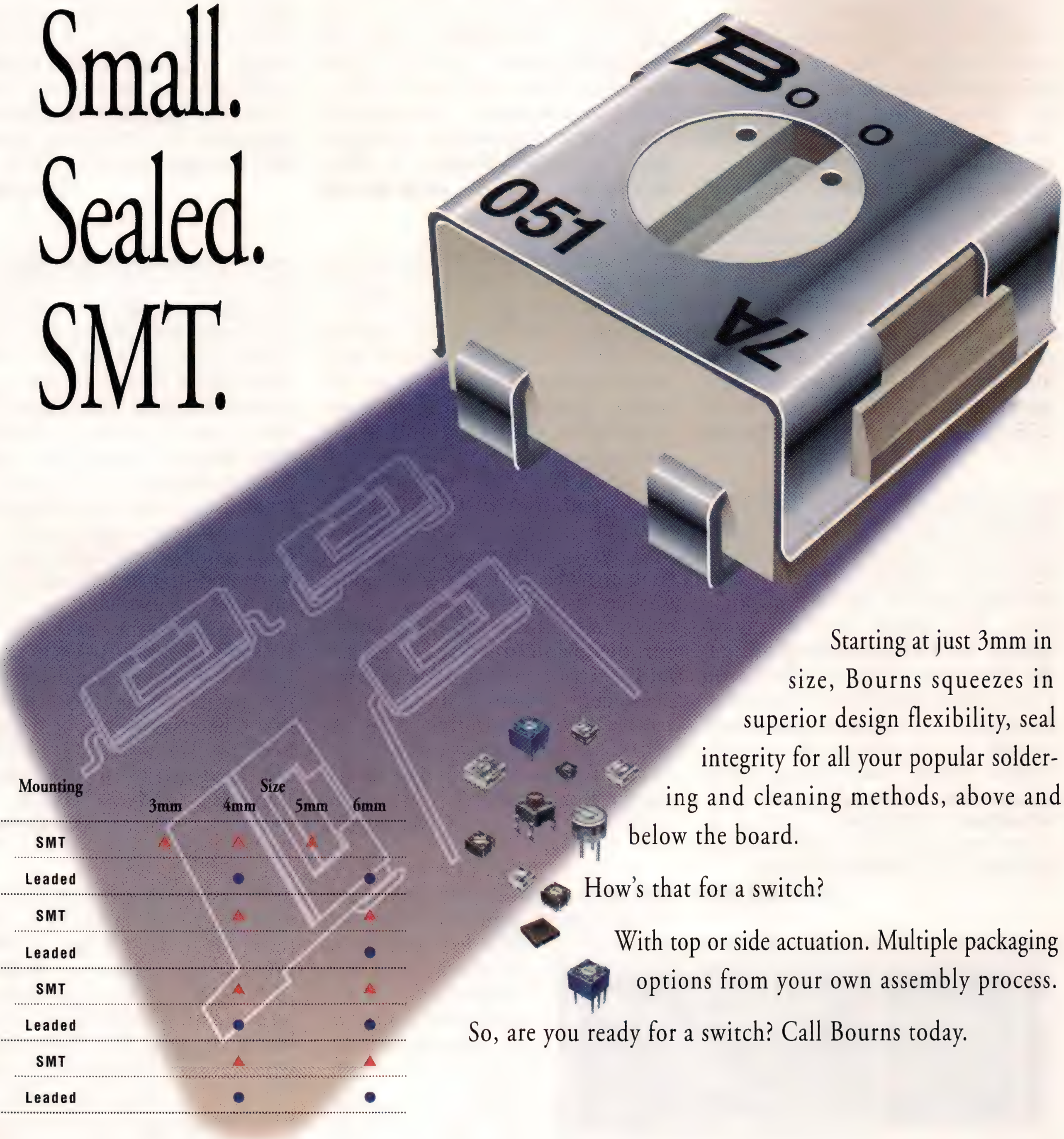

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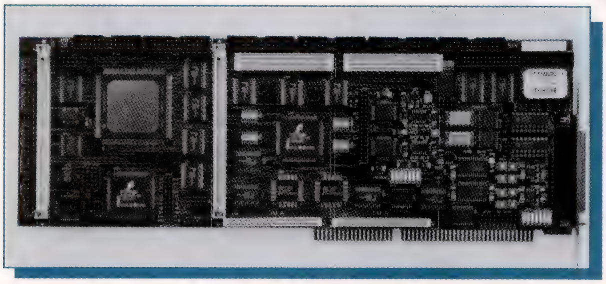
CIRCLE NO. 34

**Software invisibly weaves a digital bit stream into analog PCM samples.** The InvisiLink telecomm-software package merges a 4800-bps to 16-kbps bit stream into a standard PCM-encoded telecomm bit stream and separates the streams at the receiving end. The technique employs compression/decompression algorithms and passes all signaling, voice, fax, and modem frequencies. InvisiLink is available for the TMS320C31 DSP and costs $500 per channel (1000) for the software and the 320C31-based IndustryPack modules (one per channel), which implement the algorithm. **DSP Software Engineering Inc, Bedford, MA. (617) 275-3733.** **Circle No. 465**

**Free macro libraries fit 50-MHz FIR filters into FPGAs.** The Xilinx advanced module is a set of FIR-filter-macro libraries that provide building blocks for DSP applications. The designs are for the company's XC4000 field-programmable-gate-array (FPGA) series. You can program the filters for lowpass, bandpass, or highpass operation simply by changing filter coefficients. Filters built using these macros run much faster than software-based FIR filters running on conventional DSPs. **Xilinx Inc, San Jose, CA. (408) 559-7778.** **Circle No. 466**



**ISA card carries two C44 DSPs and 2M words of SRAM.** The PC44 combines an instrumentation-grade 16-bit analog front end, one TMS320C44 DSP, and 2M words of 32-bit SRAM. The board also accepts two TIM-40 expansion cards, and one TIM-40 card can carry an additional C44. The analog front end comprises two 16-bit, 400-kHz ADCs and four 16-bit, 256-kHz DACs. The $1995 board also carries 64 digital I/O lines, five counter/timers, and six bidirectional 20-Mbyte/sec communication ports. **Innovative Integration, Westlake Village, CA. (818) 865-6150.** **Circle No. 467**

**Intel-architecture DSP kernel and development system support native signal processing under Windows.** The IA-SPOX product line delivers real-time system software and development tools for native signal processing or host-based DSPs. The $19,500 software-development kit provides you with the SPOX DSP real-time kernel; an implementation of the Microsoft resource-manager interface, called WinSpox; a native audio subsystem that provides full Windows audio services using a Pentium µP and a codec (a hardware card is included for development work); native audio libraries; an integrated debugger; C runtime libraries; and source-code examples. The IA-SPOX kernel license alone costs $12,000. **Spectron Microsystems, Santa Barbara, CA. (805) 968-5100.** **Circle No. 468**

**Windows-based development environment generates code for TI DSPs.** Code Composer and Code Composer Plus are integrated visual-development environments for developing and debugging code for the Texas Instruments C2x, C3x, C4x, and C5x DSPs. The packages are a hybrid of Microsoft's Visual C++ compiler, signal probes and scopes for visual debugging at the block-diagram level, graphical-user-interface development tools, and conventional high- and low-level code debuggers. The packages support incremental compilation, and a graphical profiling feature helps you find code bottlenecks. Each package supports one TI DSP family and costs $1250 to $3000, depending on the number of tools in the package and the DSP family supported. **Go DSP Corp, Toronto, ON, Canada. (416) 214-1919.** **Circle No. 469**

**Soft coprocessor package executes fast 32-bit floating-point algorithms.** Look-up tables help to accelerate the SCP32 mathematical subroutine libraries in the Soft coprocessor line to speeds comparable with and sometimes faster than hardware floating-point units. The libraries' functions include basic arithmetic, data conversion, logarithmic and exponential functions, powers and roots, and trigonometric and hyperbolic functions and inverses. Linkable object modules are available for the Intel x86, the Motorola 68000, the Fujitsu 930, the Sun SPARC, and the Hewlett-Packard precision-architecture µPs. Single-copy development licenses (without a production license) cost $135. **Log Point Technologies Inc, Mountain View, CA. (415) 967-3974.** **Circle No. 470**

**$89 development kit paves the way for the ADSP-2181 16-bit, fixed-point DSP with 32k words (80 kbytes) of on-chip RAM.** The ADSP-2181 EX-Kit Lite consists of an evaluation/demo board with 16-bit stereo-audio I/O, an assembler, a linker, a PROM splitter, and a simulator. The ADSP-2181 DSP combines the ADSP-21xx architecture with 16k 24-bit words of on-chip program memory and 16k 16-bit words of on-chip data memory for a total of 80 kbytes of on-chip RAM. The company will also show several new members of the ADSP-21xx DSP family at the show. **Analog Devices, Norwood, MA. (617) 461-3881.** **Circle No. 471**

British Rail

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Signalling Control U.K. has forecast turnover for the 12 months to 31 March, 1995 of some £37 million which includes fee income of some £31 million. Most of Signalling Control U.K.'s revenues come directly or indirectly from Railtrack. The business has a forecast staff level of some 680 at 1 May 1995.

Signalling Control U.K. has its headquarters in Croydon and operational units in Birmingham, Croydon, Glasgow and York. The Croydon office also manages a unit at Swanley which is responsible for site management, installation of signalling systems and associated technical support.

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CIRCLE NO. 198

**Dual C40 development system for the PC includes a Windows-based multiDSP debugger.** The Slalom-40 development system teams one or two TMS320C40 DSPs from Texas Instruments with up to 1 Mbyte of SRAM on an ISA card. The package includes the company's new Windows-based Vista-MP multiprocessor debugger for DSPs. Vista-MP includes a uniprocessor DOS debugger, a multiprocessor Windows debugger, a parallel debug manager, and sample configuration files. The Slalom-40 costs $4995 for a one-processor board with 64 kbytes of SRAM and $5995 for a two-processor board with 64 kbytes of SRAM per processor. Vista-MP costs $795 when purchased with the company's Mountain-510 emulator. For users of TI's XDS-510 emulator, Vista-MP costs $1295. **White Mountain DSP, Nashua, NH. (603) 883-2430.**

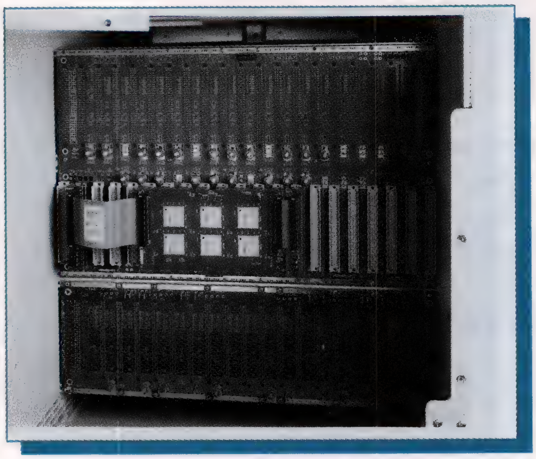
**Circle No. 472**

**Buyer's guide details DSP design tools and methodologies.** The 1995 edition of *DSP Design Tools and Methodologies: The Buyer's Guide* reports on more than 350 currently available DSP-development tools. The 800-pg book contains evaluations of these tools, and a companion volume discusses DSP design, indicating where the various tools fit in the process. $3850. **Berkeley Design Technology Inc, Fremont, CA. (510) 791-9100.**

**Circle No. 473**

**C compiler and development system for TI's C3x and C4x DSPs generate faster code.** According to the vendor, the Tartan C development system generates code for the TI C3x and C4x DSPs that is 21% faster than the most popular competitive offering. The $1495 package includes an optimizing a compiler, a runtime library, a linker, an assembler, and utilities. Tartan C/C++ generates the same tight code and allows you to code in C++. The device costs $2995. A $795 debugging-tool package is also available. **Tartan Inc, Monroeville, PA. (412) 856-3600.**

**Circle No. 474**



**Module family ties as many as 16 VME slots with as much as 1280 Mbyte/sec aggregate bandwidth.** Four additions to the Raceway Interlink module family can link as many as 16 VME slots to form an "interconnection fabric" with an aggregate bandwidth of 1280 Mbytes/sec. The modules plug onto a VME backplane, across one or more slots, over the P2 connector. Crossbar switches on the modules can connect logical channels between the slots at 70 Mbytes/sec. The ILK8, ILK12, and ILK16 modules span eight, 12, and 16 slots and cost $9900 to $13,200. An ILK1 module allows connection among VME backplanes at 160 Mbytes/sec. **Mercury Computer Systems Inc, Chelmsford, MA. (508) 256-1300.**

**Circle No. 475**

**V.17 fax protocol added to data-communications library.** The manufacturer has added the V.17 fax-modulation protocol to its SWMOD-101 data-communications library. This fax protocol supports transmissions at 7200 to 14,400 bps. The library also includes the V.21 channel 2, V.27ter, V.29, and V.33 fax protocols; the V.21, V.22, V.22bis, V.23, V.32, and V.32bis data-modem protocols; and the Bell 103, 202, and 212 data-modem protocols. Currently, the library runs on Analog Devices' ADSP-21xx DSPs. The company plans to have the library available for Texas Instruments' and Motorola's DSPs by the DSP$^x$ conference. The library is available for a fixed fee of $25,000 to $200,000 or on a royalty basis, with prices typically set at $15 to $25 per unit. **Vocal Technologies Ltd, Buffalo, NY. (716) 688-4675.**

**Circle No. 476**

**Dual-channel, 10-bit ADC board for the VMEbus operates at 70 MHz.** The Model 6472 VME board incorporates two of Analog Devices' 9060 10-bit ADCs for dual-channel, 70-MHz operation. Access to the digitized samples is through two front-panel connectors, saving bandwidth on the VMEbus. Each of the board's analog inputs accepts a ±1V full-scale signal and is terminated in a 50Ω SMA connector. A buffer amp delivers the signal to the ADC through a high-order Chebyshev antialiasing filter, limiting the input signal to approximately 30 MHz. The sample-clock generator operates at 25, 50, and 70 MHz, or you can supply an external clock through a third front-panel SMA connector. The board costs $7995. **Pentek Inc, Norwood, NJ. (201) 767-7100.** **Circle No. 477**

**Butterfly DSP takes over the Sharp LH9124 DSP and associated products.** Butterfly DSP is now handling product development and worldwide marketing of the Sharp LH9124 DSP. The chip, renamed the BDSP9124, has been placed in a ball-grid-array package and costs $490 (10,000). Development systems and faster parts will be available this year. **Butterfly DSP Inc, Vancouver, WA. (360) 892-5597.** **Circle No. 478**

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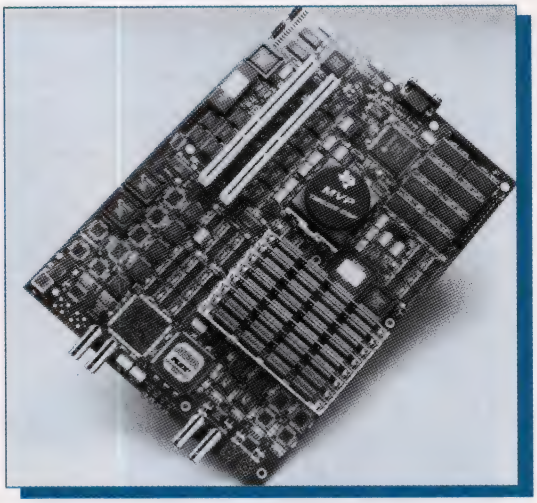
## DSP$^x$ '95 products

**Enhanced stream-driven DSP simulator generates behavioral HDL code.** Release 6.7 of the COSSAP stream-driven simulator for DSP development can generate Verilog descriptions and instantiate components from Synopsys' DesignWare library. The simulator includes direct links to the company's behavioral-compiler package and optional DSP development kits for co-simulation with the TI C5x and the AT&T 1610 DSPs. The basic COSSAP version 6.7 stream-driven simulator costs $29,000. The COSSAP HDL code generator with behavioral and register-transfer-level support costs $7500, and the DSP development kits each cost $7500. **Synopsys, Mountain View, CA. (415) 962-5000. Circle No. 479**

**$600 DSP-C31 development system supports TI C31.** The development system includes an ISA card with a TMS320C31 DSP, 32k words of 32-bit-wide SRAM, and a 14-bit codec (TLC32044) with input and output amps for the analog channels. Software includes an assembler and a symbolic debugger. **Domain Technologies Inc, Plano, TX. (214) 985-7593. Circle No. 480**

**Mistral 1 and 2 support Verilog synthesis.** Mentor Graphics has added Verilog output to its Mistral 1 and 2 high-level DSP synthesis tools. The products previously emitted only VHDL. The tools are part of the company's DSP Station suite of DSP development tools. **Mentor Graphics, Wilsonville, OR. (503) 685-7000. Circle No. 481**

**ISA board carries C32 floating-point DSPs and accepts two daughtercards.** The C32 (Loughborough's PC/C32) real-time-system board loads a 50-MHz C32 floating-point DSP with two banks of SRAM and a pair of daughtercard sites onto an ISA card. SRAM banks 0 and 1 can hold up to 128k×32 bits and 512k×32 bits of memory. The board contains a socket for a 32-kbyte boot EPROM. The board's two daughtercard sites accept analog and digital I/O cards. The product is available from Spectrum Signal Processing and Loughborough Sound Images. Spectrum sells the card starting at $1495, depending on memory. **Spectrum Signal Processing Inc, Burnaby, BC, Canada. (604) 421-5422. Circle No. 482**
**Loughborough Sound Images Plc, Loughborough, Leicestershire, UK. (44) 0 509 634300. Circle No. 483**



**Master development board features the C80 MVP DSP.** The Master development board, the TI TMS320C80 MVP, is a 2-BOPS (billion operations/sec) multiprocessing DSP. The board contains up to 24 Mbytes of SRAM, as many as four 330-Mbps serial links, a video controller, 4 Mbytes of VRAM, a 512-kbyte EPROM, and two 64-bit PCI expansion connectors. For software development, the board connects to a Sun workstation through a TI XCS-510 emulator using its Joint Test Action Group emulation port. The board costs $6950 to $11,480, depending on configuration, plus $390 per megabyte of SRAM. **Wintriss Engineering Corp, San Diego, CA. (619) 550-7300. Circle No. 484**

**Multichannel TIM-40 image-processing module accepts line-scan inputs.** The MDC40IL line-scan image-processing module accepts signals from one digital or four synchronous analog line-scan cameras and employs a C40 DSP for image processing. The device digitizes the incoming video at software-programmable rates to 20 MHz. The card also accepts as much as 512 kbytes of SRAM and 16 Mbytes of DRAM for large image-processing applications. The card plugs into a standard TIM-40 socket but physically requires two adjacent TIM-40 sites. The product is available from Spectrum Signal Processing and Loughborough Sound Images. Spectrum sells the card starting at $5245, depending on memory. **Spectrum Signal Processing Inc, Burnaby, BC, Canada. (604) 421-5422. Circle No. 485**
**Loughborough Sound Images Plc, Loughborough, Leicestershire, UK. (44) 0 509 634300. Circle No. 486**

**Parallel C version 2.0 for the C40 debuts.** 3L has announced the latest version, 2.0, of its $4500 Parallel C compiler for the C40 DSP. **3L Ltd, Edinburgh, Scotland, UK. (44) 31 662 4333. Circle No. 487**

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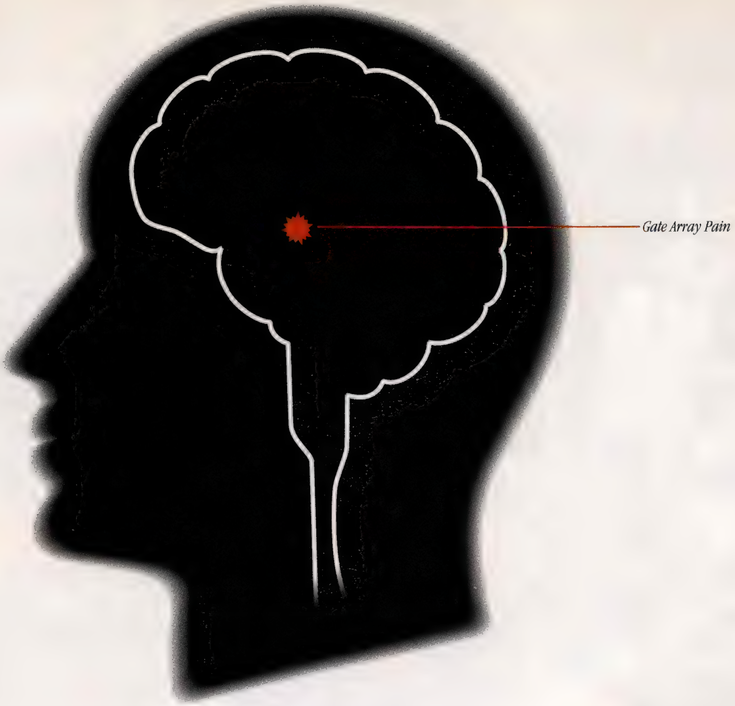

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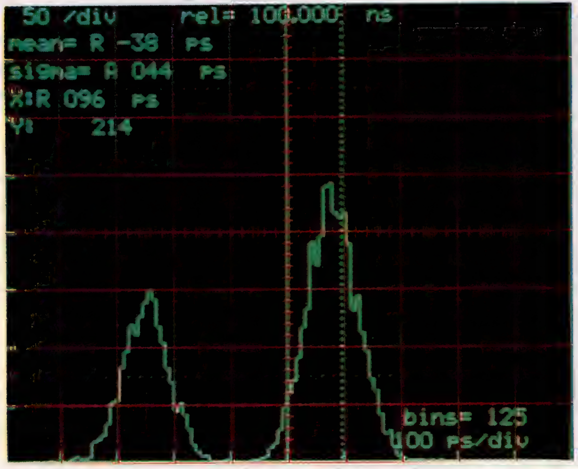

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# Gain control goes silicon

BILL SCHWEBER, TECHNICAL EDITOR

**Increasingly, ICs are replacing mechanical potentiometers for gain control, providing both flexibility and compactness. However, you must choose carefully from among available architectures. Incompatibilities, limitations, and unique architectures complicate the final choice.**

If you think circuit gain adjustment is just an annoying artifact from the predigital era, think again. A properly ranged signal is still necessary for maximizing system S/N ratio, for matching source and load, and for reducing error rates and distortion. Many systems need gain or parameter adjustment for a variety of functions—from controlling volume, screen brightness, and filter settings to automatically maintaining system performance during changing conditions.

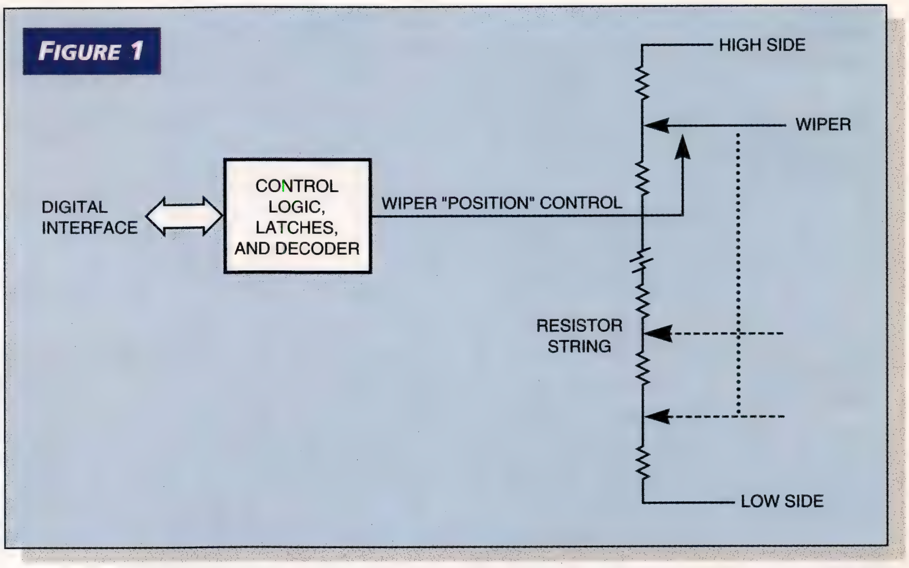
The implementation of gain control has changed, however. Traditional mechanical trimming potentiometers face a strong challenge from their silicon equivalent, digital, or electronic, trimmers. Digital trimmers offer flexibility, reliability, freedom from mechanical hysteresis, and compactness compared to their electromechanical predecessors. But, differences among vendors in internal architecture, specifications, and interfacing make it difficult to choose the "best" device for your application (see **Table 1**).

Also, applying an active component to replace a passive trimming potentiometer is not a simple swap. The digital trim also involves a new set of parameters, including volatility, power-handling, and noise. As a result, you may want to delay jumping on the digital bandwagon. Consider alternative approaches, such as mechanical trimmers (see **box**, "Don't ignore the mechanical trimmer") and multiplying DACs (see **box**, "MDACs: another alternative").

Fortunately, electronic trimming via digital pots opens new approaches to solving traditional calibration issues. You can perform automated system calibration, both on power-up and during system operation. But you should also view calibration and adjustment in a new light, because digital pots provide more—and more accessible—adjustment points than do mechanical devices. If you use digital devices to their maximum potential, you can put "operator adjustment," "opportunity for misadjustment," and "excessive tweaking" on your list of former problems.

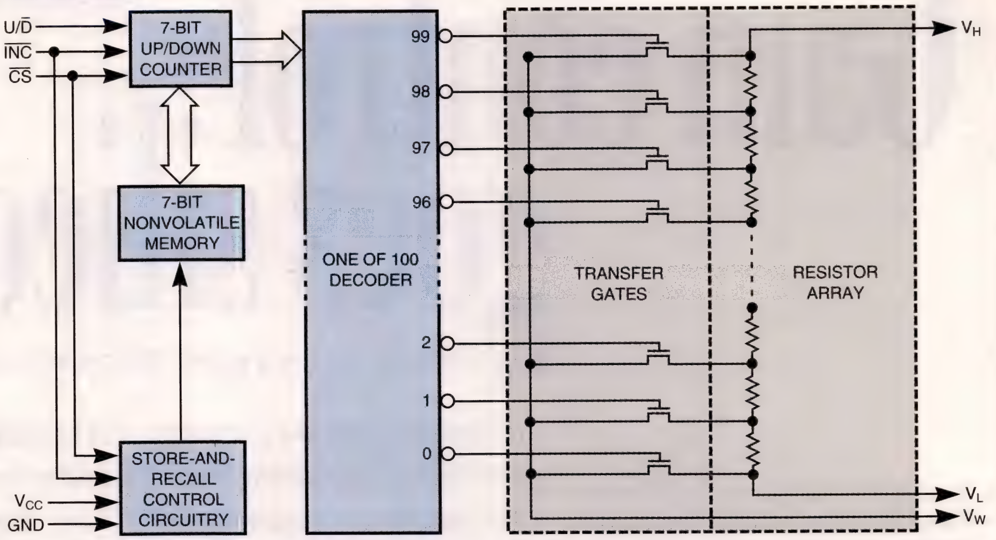
The core of a digital pot comprises a

**FIGURE 1**



**A digital pot comprises a string of resistors with FET switches, controlled by onboard logic and decoders, between each resistor pair.**

FIGURE 2



**Xicor's nonvolatile X9312, with 99 resistors (100 positions), has three control lines: an up/down line for setting increment direction, a line for stepping, and a chip select.**

series string of resistors, with the connections between resistors tapped to a wiper via an FET switch (**Fig 1**). Relatively simple control logic manages the necessary switching. As you turn the switches on and off, you observe the same effect as that of a wiper's changing resistor positions or turns to reach a desired tap.

Digital pots offer some obvious advantages over mechanical trimmers. For example, the digital devices lack moving parts and offer greater mechanical ruggedness and vibration resistance. They come in standard DIP or surface-mount IC packages, and you can install them with standard equipment and handle them as you would any other IC. The advantages go beyond the basic package and ruggedness, however. Digital pots are available in 2-mm-high packages, making them compatible with low-profile formats, such as PCMCIA Type I cards. In addition, 1-mm-high TSSOPs will be available soon. Single, dual, and quad digital pots in a single package also make maximum use of limited pc-board space.

Digital pots also change the way you

## TABLE 1—REPRESENTATIVE DIGITAL POTENTIOMETERS

| Company | Model | Steps | Resistance (kΩ) | Configuration | Nonvolatile | Packages | Interface | Operating power | Features | Price (1000) |
|---|---|---|---|---|---|---|---|---|---|---|
| **Analog Devices Inc**<br>**Circle No. 301** | AD8402 | 256 | 10, 50, 100 | Dual | No | DIP-14, SO-14 | Three-wire | 2.7 to 5.5V, 5 μA | Full ac specs, nA shutdown current | $1.66 |
| | AD8403 | 256 | 10, 50, 100 | Quad | No | SOL-24 | Three-wire | 2.7 to 5.5V, 5 μA | Full ac specs, nA shutdown current | $2.51 |
| **Dallas Semiconductor Corp**<br>**Circle No. 302** | DS1267 | 256 | 10, 50, 100 | Dual | No | DIP-14<br>SO-16,<br>TSSOP-20 | Three-wire | 5 or ±5V, 650 μA | Stackable wipers for 512-step resolution | $2.45 |
| | DS1867 | 256 | 10, 50, 100 | Dual | Yes | DIP-14,<br>SO-16,<br>TSSOP-20 | Three-wire | 5 or ±5V, 650 μA | Nonvolatile version of DS1267 | $3.14 |
| | DS1802 | 64 | 50 | Dual | No | DIP-20,<br>SO-20,<br>TSSOP-20 | Three-wire and pushbutton | 3 or 5V, 2 mA | Log taper, mute, audio specs | $2.56 |
| **Xicor Inc**<br>**Circle No. 306** | X9511 | 32 | 1, 10 | Single | Yes | DIP-8,<br>SO-8 | Pushbutton | 5V, 3 mA<br>200 μA standby | Auto-store or user-store wiper, X9514 is a log-taper version | $0.85 |
| | X9221 | 64 | 2, 10, 50 | Dual | Yes | DIP-20,<br>SO-20 | Two-wire ($I^2C$-compatible) | 5V, 2 mA<br>500 μA standby | Multiple wiper settings, can be cascaded | $2.80 |
| | X9312 | 100 | 1, 2, 10, 50 | Single | Yes | DIP-8,<br>SO-8 | Three-wire | 5V, 3 mA | Up to 0 to 15V across terminals, up/down, clock select 1-mA shutdown | $1.45 |

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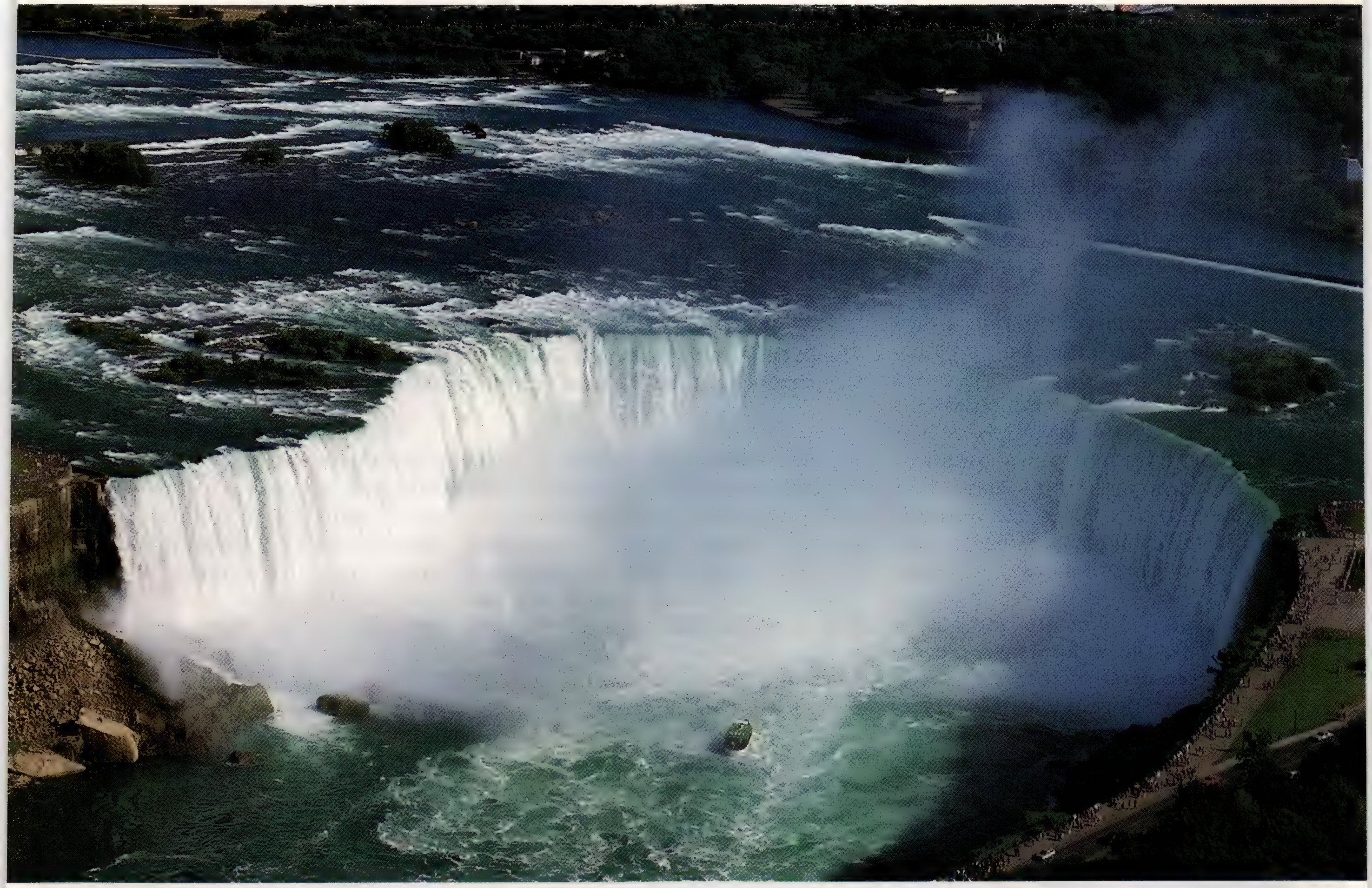

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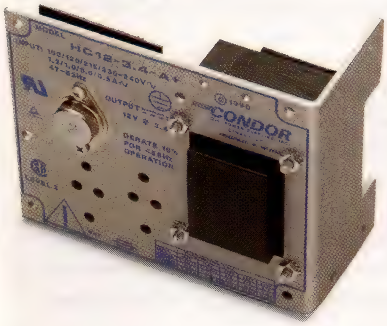

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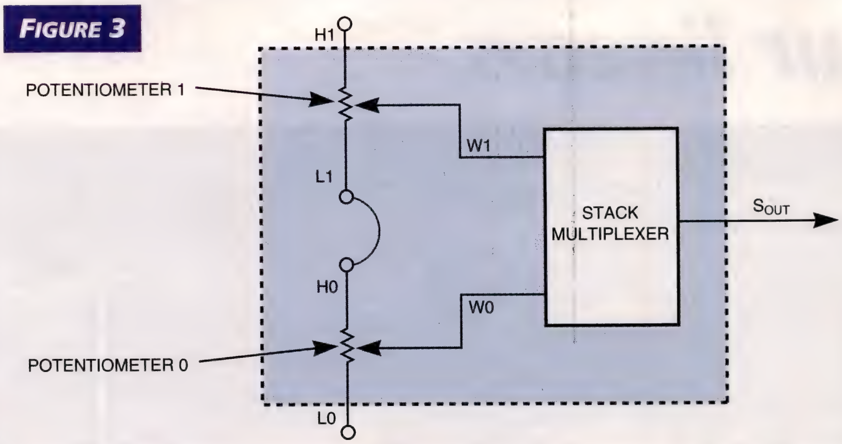
design trims into a circuit. A traditional approach groups multiple trims at one board edge for convenient operator access, except what is convenient or necessary for an operator often degrades circuit performance and takes up board space. With digital pots, instead of placing the trim to ensure reasonable access for the person doing the trimming, you can place the trim close to its associated circuit. This approach yields better signal-integrity maintenance, reduced noise pickup, and reduced use of the board space a mechanical trim requires to run tracks to remote trims.

The direct approach to using a digital pot to replace a mechanical potentiometer is on a one-for-one basis. Before you do that, carefully study the specs of these active devices to see how they differ from mechanical trimmers. Equally important, think about how you use trims to see if using a software-controllable trim changes the way you achieve your performance goal in the circuit.

For example, you no longer need compromise the performance to avoid complex or iterative trim sequences. Unlike a test operator or technician, these sequences don't irritate the algorithm that controls them. Similarly, you need not reduce trim-adjustment locations solely to reduce operator test and trim time if an extra trim would provide performance benefit. You can design a circuit that will more easily tolerate system test and calibration on the production floor. Finally, the ability to trim and set gain, offset, and operating points during circuit operation means that you can design a circuit that adapts to changing conditions and configures itself under software control for best performance in the signal path.

**FIGURE 3**



**The DS1287 (and nonvolatile DS1867) features an internal multiplexer so that its two channels can be "stacked" to provide twice the resolution of either channel.**

### Not drop-in replacements

Digital pots need power to operate, so you must consider some complex issues, such as how they retain and restore wiper settings when you remove and reapply power. Vendors offer various solutions. For example, the 100-step Xicor X9312 digital pot has built-in nonvolatile, electrically erasable memory (**Fig 2**). You can set the device to retain the last wiper position when you remove power and restore it when you apply power. Alternatively, you can set the device to power up to a preset value. This approach would suit applications in which the device controls audio volume, for example, so that sound level doesn't come up at full blast when you restore power. Similar-

## DON'T IGNORE THE MECHANICAL TRIMMER

Mechanical trimming potentiometers, available from such vendors as Bourns and Spectrol, have served circuit designers well for decades. A single-turn pot provides resolution, which differs from repeatability, of about 0.05%, or one in 200 parts; multiturn pots offer greater resolution. Before you rush out to replace a trimmer with a digital pot, consider some of the virtues of this old friend.

For example, trimmers come in a range of values from a few ohms to megohms, and their power-handling capabilities are limited only by how much space your circuit has. They also provide flexibility: You can easily change your design's installed resistance value. Further, mechanical trimmers can withstand greater overloads and common-mode voltages than do digital pots; the circuit supply voltage puts less constraint on the mechanical devices' signal level.

In addition, because of their lower parasitic capacitance, mechanical trimmers generally have wider bandwidths than do digital pots. You can also adjust mechanical trimmers without operating-system software, drivers, or debuggers. All you need do is apply power and signal to your circuit and monitor a test point with appropriate equipment, such as a scope or meter. This approach is convenient for adjusting an analog-signal chain for gain/offset/range parameters or for setting up an analog filter.

By measuring resistance with a meter, you can easily determine whether a mechanical trimmer is working properly. You need no applied power or software. In addition, you need not worry about your software's changing a setting that you want set for the lifetime of the equipment. Also, application software does not have to manage settings.

Unlike digital pots, nearly every mechanical device is available from several second sources. Finally, because trimmers are nonvolatile, they avoid all the power-on and write-cycle issues of digital pots.

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ly, the Analog Devices AD8402 series and the Dallas Semiconductor DS1668 series power up at vendor-preset positions.

Not all applications require nonvolatile storage of the wiper setting. To meet these needs, Dallas Semiconductor offers both volatile and nonvolatile devices; for example, the DS1867 is the nonvolatile version of the DS1267 256-position dual digital pot. Analog Devices minimizes digital pot complexity and cost by assuming that you can use some other nonvolatile memory in the your system.

As always, you must make the trade-offs in component cost, allocation of power-up functions (system software vs the IC's transparent internal memory), and desired power-up condition (using the last pot setting, a software-defined value, or a trimmer-defined neutral, or midscale, setting). For digital pots without internal memory, consider the implications on your production or field-test operation when you store the trimmer setting in a component that is physically separate from the trimmer IC.

Consider the application and the number of times the setting of the trimmer will change and, thus, require storage. The EEPROMs in digital pots perform 50,000 to 100,000 writes, probably enough for most applications, and data retention is more than 100 years—well beyond the equipment's lifetime.

Vendors and models offer different approaches to how and when to store the pot settings—another source of potential confusion and functional incompatibility. You can set the Xicor X9511 to store the current setting whenever you remove power; you can also set the device to store any changes in wiper setting as they occur. The Dallas Semiconductor DS1869 uses a different approach: It automatically stores a new setting if the change is greater than 12.5% of the total resistance range.

Also, consider what you want to happen if you shut down power while the wiper position is changing. Should the memory retain the last "valid" position (when a time-out indicates that the wiper has stopped moving), or could you inadvertently show some indeterminate value? Finally, watch how your power supply drops when you remove power. For the EEPROM to automatically store on power-down, the rail must drop slowly enough so that there is time to both sense the drop and to perform the write cycle. Carefully check the data sheets and your design to ensure that the power-supply drop-off rate meets the specification.

### Pick a value, but not any value

Unlike mechanical trimming pots, digital pots don't offer a large span of full-scale-resistance values. You must properly scale your associated circuitry to make maximum use of a digital pot's values. All vendors offer 10-, 50- and 100-kΩ nominal values; Xicor also offers some 1- and 2-kΩ units.

You must also consider resolution. Vendors specify digital pots by the number of distinct positions, or taps, they provide. This number ranges from 32 to 256, and some devices, such as the Dallas DS1287 or DS1867, can cascade,

## MDACs: ANOTHER ALTERNATIVE

Multiplying DACs (MDACs) are functionally similar to digital pots, providing a usually buffered output current or voltage equal to the input signal multiplied, or weighed, by the digital setting of the DAC input. Rather than a series string of switched-in resistors, however, MDACs use R-2R ladders to assign weights on the input signal. MDACs take a variable static or dynamic external analog signal as their reference instead of using a fixed reference value to the R-2R ladder. Most MDACs buffer the input as well.

MDACs can support either two-quadrant multiplication, with the input spanning from negative to positive and the control signal positive only, or four-quadrant multiplication, with the input and control both spanning negative to positive. MDACs offer resolutions of 8, 12, 14, and even 16 bits. Traditionally, MDACs were available only with parallel interfaces, but many new units feature serial interfaces for smaller package size, as well two, four, and eight channels in a single IC. Most MDACs let you set the output buffer to provide gain and attenuation.

As voltage- or current-output devices, MDACs would not suit an application requiring variable resistance. However, you may consider them for applications controlling or setting a voltage or current value. These applications include controlling programmable power supplies, establishing dc or bias conditions for op amps, adjusting digitally controlled analog filters, and setting gain or power levels for amplifiers, as well as providing comparator setpoints in automatic test equipment.

Application-specific MDACs for high-fidelity-audio volume control provide such features as stereo operation (two linked channels), panning (increasing one channel's gain while reducing the companion channel's gain), muting, tone (treble and bass), and balance. These MDACs cover the audio bandwidth. For example, the TDA7312 from SGS-Thomson Microelectronics lets you choose one of four stereo-input channels, control in 1.25-dB/step, and control via the I²C bus µP interface. National Semiconductor's LM1972, an audio-specific, dual R-2R resistor string offers 70-dB attenuation (0.5-dB steps from 0- to 47.5-dB attenuation and 1-dB steps from 48 to 104 dB, along with mute. You control the device with a three-wire serial interface that you can daisy-chain to as many ICs as necessary.

Other MDACs, such as the Maxim MAX532, are 12-bit devices for dc-level setting, which you can use for controlling programmable power supplies and in other test applications. These devices emphasize dc specs, such as integral nonlinearity, gain TC, settling time, and guaranteed monotonicity over temperature. However, some, such as the AD7845, also provide ac specs, including full- and small-signal bandwidth, along with THD.

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or stack, digital pots to achieve greater resolution, with 256 taps achieving approximately 0.4% resolution (**Fig 3**). But many applications, such as setting screen brightness or adjusting an analog signal-path gain range, don't require high resolution, and 32 taps may be enough.

The steps between taps also need not be linear. Both Xicor and Dallas offer log steps for applications, such as audio volume, having wide dynamic ranges in the signal. The Dallas Semiconductor DS1802 features 64 steps with 1-dB/step log taper; the Xicor X9514 has 32 log steps.

Just as with any other pot, you can use these digital pots in two modes: three-terminal, voltage-dividing, or ratiometric, potentiometer mode or two-terminal, simple-resistor, rheostat mode. When using the pots as a rheostat, tolerance from nominal can reach 20%. However, many applications, especially those using the pots as voltage dividers, don't require low tolerance.

Designing with digital pots also offers good channel-to-channel matching on multiple-channel devices. For example, the Analog Devices AD8402 family has 1% matching. Digital devices also provide good matching temperature coefficients: Although rheostat's temperature coefficients of resistance (TCRs) can reach 500 ppm/°C, those of resistive dividers can be as low as 15 ppm/°C.

### Setting the values you want

You can set a digital pot's value through a processor interface or a "switch-closure" interface. Processor interfaces are serial to minimize interconnection requirements for clock, data, and chip select. Interfaces and timing differ, however, reducing your design's ability to accommodate multiple sources. Maximum clock rates range from 1 to 10 MHz, so you must provide a corresponding clock in your system.

Most digital pots use internal, nonvolatile memory as "shadow" memory, which transparently saves new settings by sensing the power-down transition. Others use the system processor to write to an EEPROM register, which, in turn, controls the wiper; this approach has more complex system timing and protocol requirements. Some Xicor devices support a bidirectional master/slave protocol over the serial data line. In this approach, the digital pot acts as a slave to acknowledge handshaking to the master CPU to verify that it received valid data.

Serial interfaces can be absolute-position or up/down versions. In absolute-position interfaces, you load a word with the desired wiper-position number. In up/down interfaces, you select up or down mode and issue pulses to step the wiper through succeeding positions. Digital pots having multiple channels on one IC reserve extra data bits to indicate which internal channel is being addressed.

You can daisy-chain some serial absolute-position devices via a data-out signal connected to the data in the signal of the next device. This lets you control a virtually unlimited number of pots via just three wires, and double-buffered latches prevent the pots from responding to transitional data bits.

However, a processor algorithm does not make all trims and adjustments in a circuit. For example, users typically set screen brightness and volume control. In these cases, you may not want to involve a processor in the adjustment loop such that the processor would have to interpret a user's finger action and send a corresponding command to the affected part of the circuit.

Switch-closure interfaces suit applications, such as volume, brightness, and temperature control, requiring hands-on adjustment. In these applications, changing the resistor value directly affects the final signal you want to control, independent of a processor action or software. Both Dallas Semiconductor and Xicor offer units with debounced lines for the up and down pushbutton connections. The Xicor X9511 PushPot and its log-taper sibling, the X9514, exemplify digital pots that let users directly set a value via two pushbuttons.

Consider what your design can tolerate while a wiper is changing. Because digital pots include on/off switches that connect each resistive element, consider what happens if one switch makes or breaks before the next switch breaks or makes. Momentary glitches occur when the apparent resistance value suddenly makes a large step before settling to the desired value. Again, this consideration may be irrelevant in such applications as brightness control. However, in other applications, such as channel gain ranging, such glitches can cause signal overrange and input saturation, which you must accommodate via suitable timing. Some new devices, such as the Analog Devices AD8402 series, contain circuitry to minimize any glitches inherent in

## MANUFACTURERS OF DIGITAL POTS AND MDACS

For free information on the digital pots and multiplying DACs (MDACs) such as those described in this article, circle the appropriate numbers on the postage-paid Information Retrieval Service card or use *EDN*'s Express Request service. When you contact any of the following manufacturers directly, please let them know you read about their products in *EDN*.

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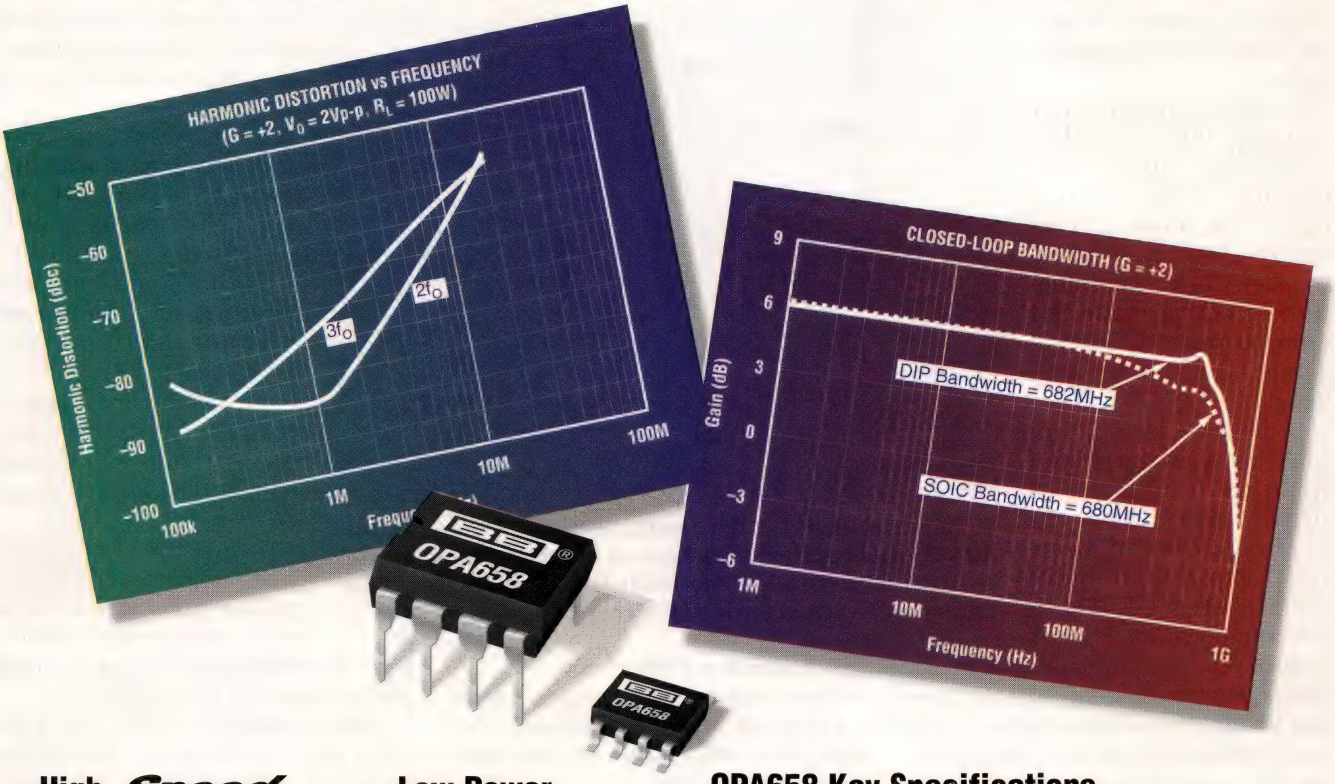

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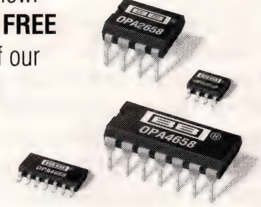

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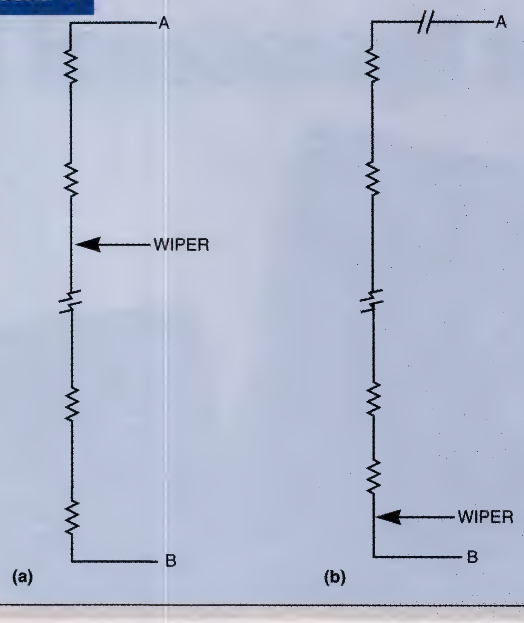
CIRCLE NO. 171

switched-resistor designs. The Dallas Semiconductor DS1801 for audio features zero-crossing detection circuitry, which eliminates "zipper" noise by allowing the wiper to move only during moments of no audible signal.

The trend toward lower voltages and power has reached these digital components. Some devices operate on single 3 to 5V supply; others, on dual ±3V supplies. Current consumption in active mode has dropped from 10s of milliamps to just a few milliamps.

Some new devices consume just a few microamps when in shutdown or standby mode, which differs from power-off mode. For example, you can put the AD8402 series (**Fig 4**) into shutdown mode via a control pin. The pin makes the device open one of its internal resistor-string-end terminals while shorting the wiper to the other terminal and while retaining the wiper setting in internal latches for use when leaving shutdown mode. As a result, the only current consumption is a 5-µA leakage in the resistance string.

**FIGURE 4**



**In shutdown mode (a), the resistor output of Analog Devices' AD8402 changes from the power-on position to one terminal open (b), with the wiper shorted to the other terminal, while retaining the actual setting in latches.**

Typically, you need not worry about a mechanical trimmer's wiper. With digital pots, though, you must limit wiper current to less than 1 mA. You must also consider wiper resistance, which can range from 40Ω to several hundred ohms. Higher wiper resistance reduces temperature stability and bandwidths.

You must also limit the applied signal span. Typically, you have to keep the maximum analog signal across the ends of the resistor string within the supply voltage, with a little extra head room. Xicor's X9312 allows 0 to 15V across its terminals from a 5V supply. Applied signal span can be a problem if your system has transients or if you don't have complete control over the applied signal, such as one from an external source.

### Specs make a difference

Digital pots are functionally simple, but, like all other components, they have subtle performance specifications. Unfortunately, differences in vendors' internal architectures, interfaces, and approaches mean that data-sheet formats and specs have little in common. Some concentrate on digital control and timing; others emphasize analog performance through the resistor string. You must carefully examine such specs as bandwidth, linearity and distortion, dynamic signal handling, crosstalk, and internally generated noise, for example.

Bandwidth ranges from audio frequencies to about 1 MHz. For example, the 1-kΩ Xicor XC102 in rheostat mode has a 1.8-MHz, –3-dB point. However, RC time constants largely determine bandwidth, and the 10-kΩ family member has a 30-kHz bandwidth. In contrast, the 10-kΩ AD8402 features 600-kHz bandwidth. Some devices suit audio volume controls, providing flat response and full specs over the 20-kHz audio band.

Linearity and distortion are important in such applications as audio signals and critical open-loop settings. A well-designed device can provide internal noise level and differential nonlinearity comparable to those of D/A converters: 2 and 1 LSB, max, respectively. Similarly, several models offer distortion below 0.010% for the audio band.

Carefully check the specs for dynamic signal handling. Again, this feature is not important in digital pots in level-setting applications, such as brightness, but is necessary in those applications in which the digital pot must pass ac signals.

Not all devices have a crosstalk spec. Crosstalk between channels in multiple channel devices is typically –60 dB or better.

The resistive elements and wiper resistance contribute to internally generated noise, which may be significant at high bandwidths switching in lower position resistors in the string.

Careful attention to these specs will affect the success of your design: Pay attention beforehand so you won't waste time—and money—with the wrong device.

## Acknowledgments

*Thanks to Walt Heinzer of Analog Devices Inc, Paul Nunn of Dallas Semiconductor Corp, and Gray Creager of Xicor Inc for their help and insight.*

*You can reach Technical Editor Bill Schweber at (617) 558-4484; fax (617) 558-4470.*

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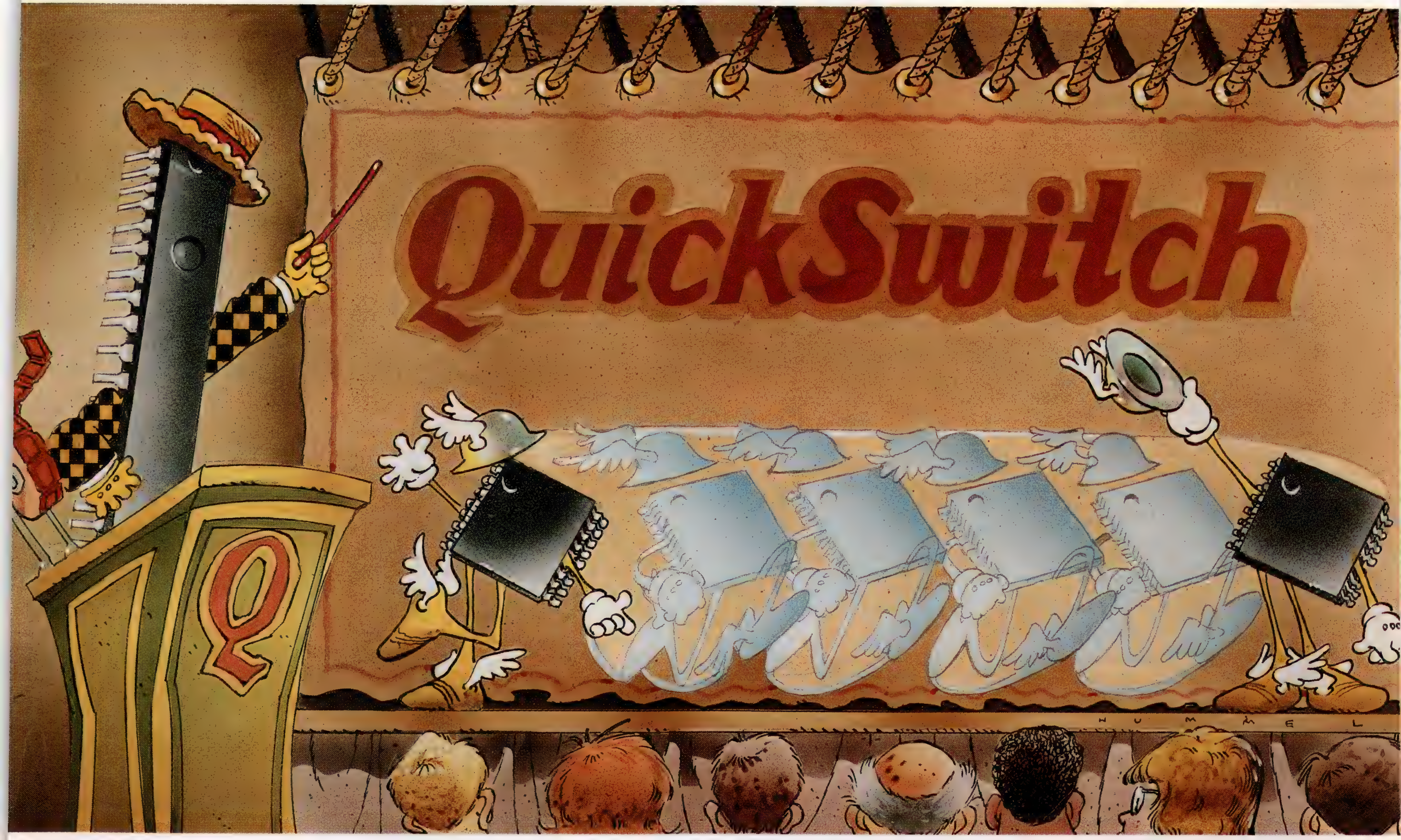

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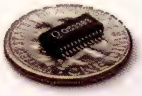

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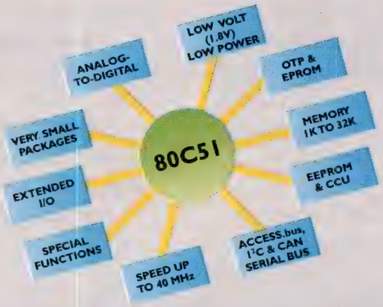

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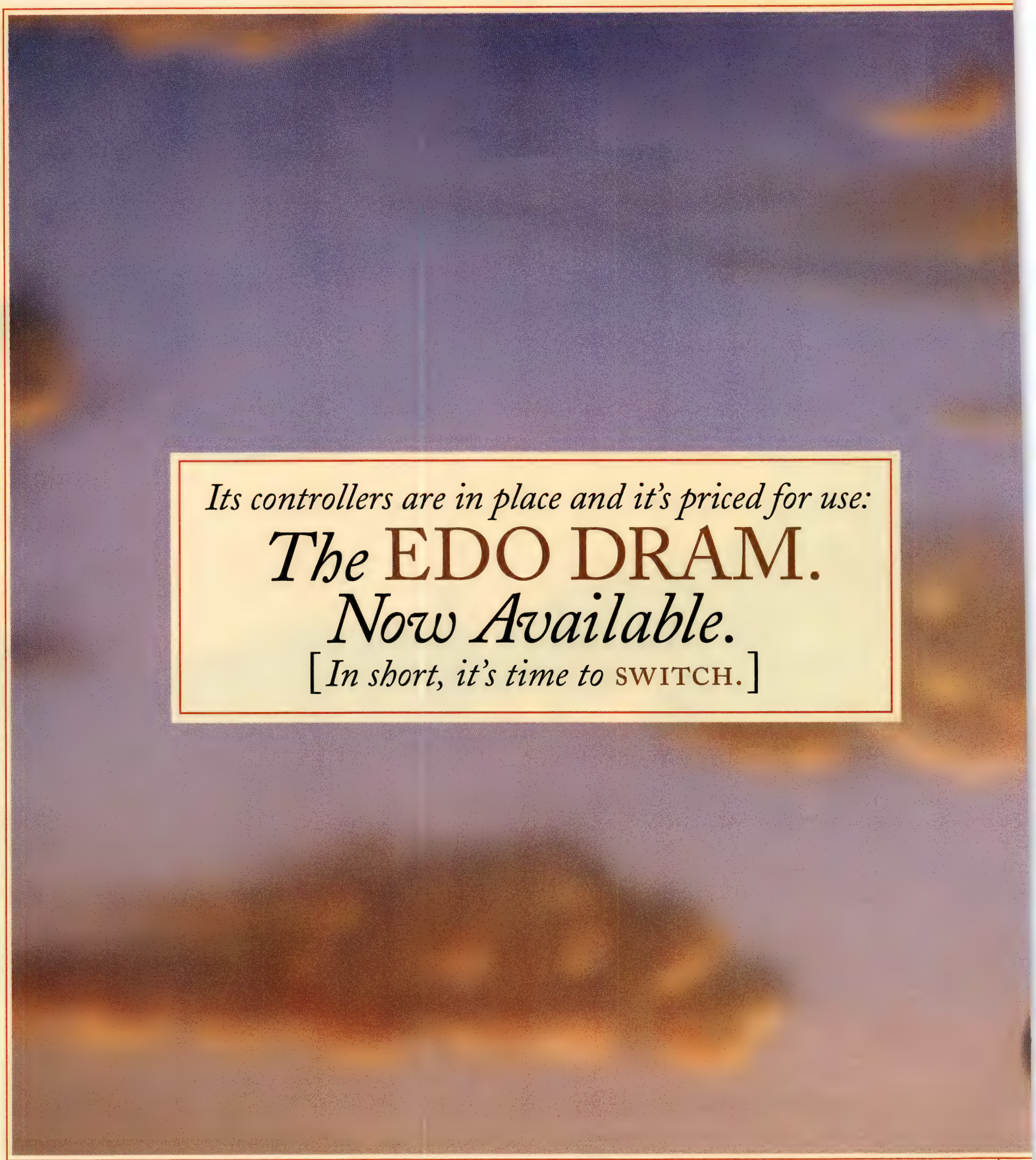

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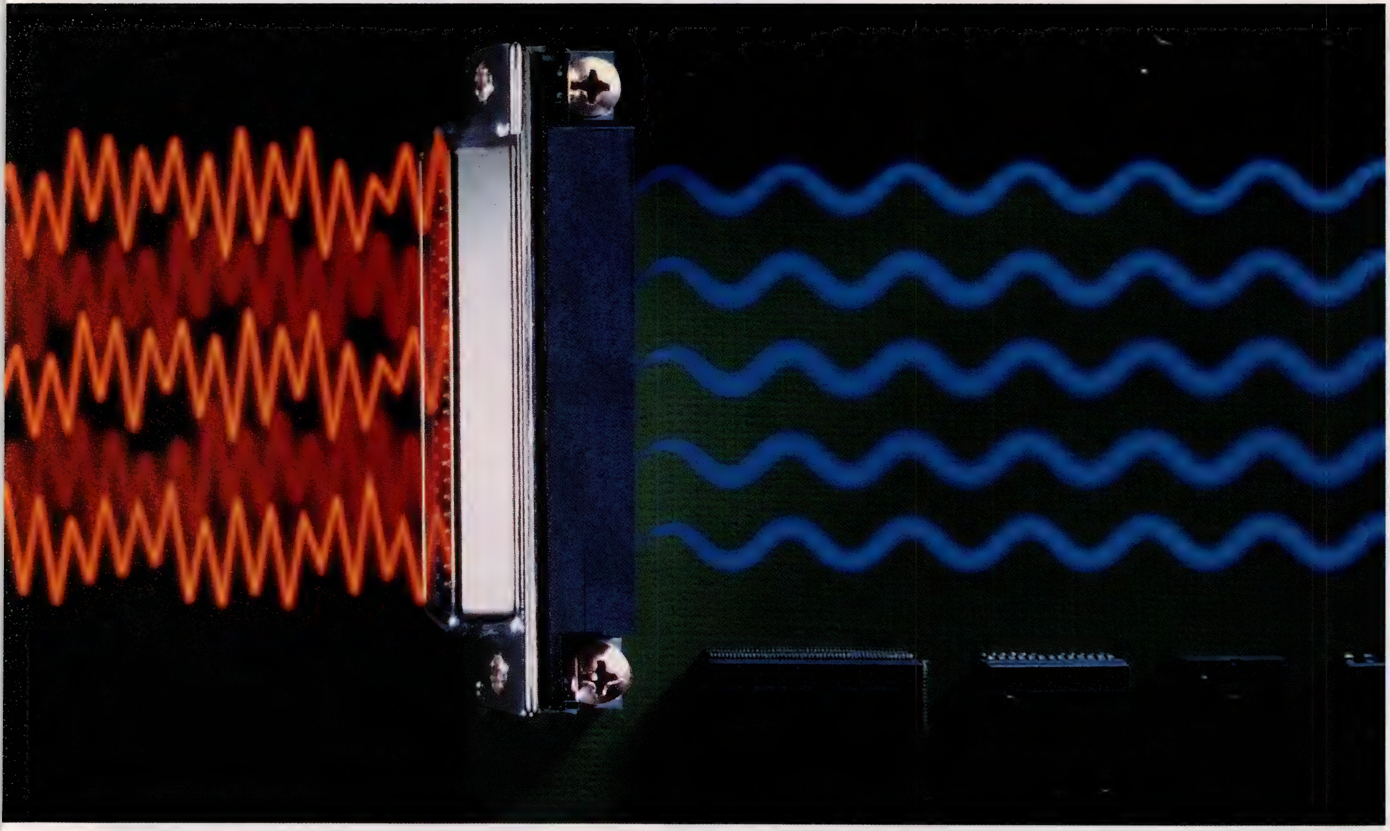

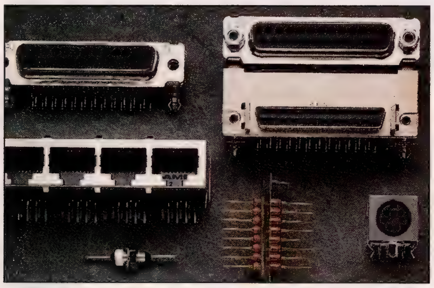

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CIRCLE NO. 3

AMP

# Old-dog 555 learns six new tricks

**JAMES KEITH, IMD FINCOR ELECTRONICS DIVISION, YORK, PA**

The circuits in **Fig 1** invert the ubiquitous 555 timer's operation. The circuits' output polarities are the inverse of conventional 555 timers'. The circuits' output duty cycle is exactly 50%. Further, you have a choice of open-collector or totem-pole output—or both. And you can feed the timing capacitor from a negative current source referenced to the circuit's common.

I recommend the Texas Instruments TLC555, but any 555

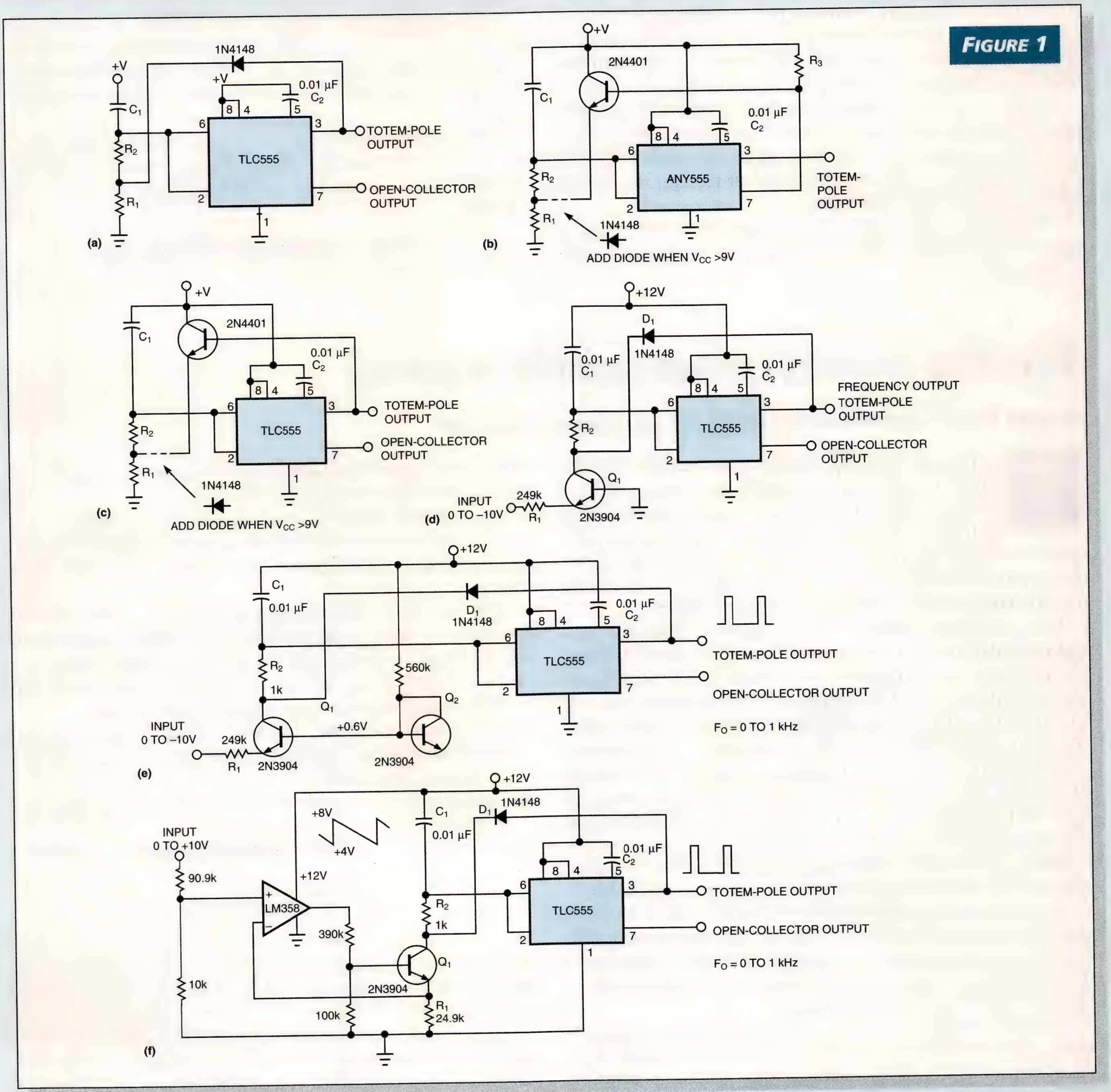
**FIGURE 1**

**You can configure an "inverted" CMOS 555 timer as a free-running oscillator (a), an inverted bipolar 555 with active reset (b), an inverted CMOS 555 with active reset (c), a simple VCO (d), an improved version of the VCO (e), and a VCO sporting an amplified current source (f).**

timer should work. The TLC555 has the advantage of being CMOS. Its low power consumption does not introduce switching spikes into the power supply. The TLC555's output also tends to saturate better in the positive direction than devices from other CMOS 555-timer vendors. This feature suits the TI device better for this application.

One disadvantage of the TI device is its limited output-sourcing capability, which limits the capacitor-reset current to 10 mA max. On the other hand, this limitation could be an advantage under some conditions if you use the current-limiting property to eliminate the reset-resistor, $R_2$.

In the circuits, the timing capacitor, $C_1$, ties to the positive bus to keep its discharge current out of the power supply. However, connecting $C_1$ to the negative bus causes the 555 timer to wake up with an opposite-polarity output—a little-known feature of the 555 timer.

The circuits simply bypass the timers' pin 5, the control input. The control input is the top node of the 555's internal voltage divider. In these circuits, bypassing this node to $V_{CC}$ via $C_2$ stabilizes the devices' upper threshold. But the lower threshold is at the mercy of the power-supply bus. Therefore, I recommend bypassing the power supply with a healthy sized capacitor to minimize jitter induced in the 555's lower threshold. This extra capacitor is one disadvantage of these configurations.

The low-voltage operation of the circuits is surprisingly good. The circuits that employ a TCL555 operate easily at 5V. A Schottky diode could further enhance low-voltage operation at the expense of increased diode leakage—a possible problem.

In the sixth circuit, you must use a well-regulated supply because the 555's bandgap reference operates from a voltage divider. Such a setup has *no* power-supply rejection. (DI #1694)

**To Vote For This Design, Circle No. 324**

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# Algorithm converts random variables to normal

***EDWARD BEADLE, BROOKHAVEN NATIONAL LABORATORY, UPTON, NY***

Although *normally* distributed random variables are essential for many engineering analyses, software packages usually provide only a function that generates *uniformly* distributed random samples over the range [0,1]. However, a simple algorithm allows you to convert the uniformly distributed samples into normally distributed samples to a very good approximation.

The algorithm repeatedly takes N samples from the uniform distribution, sums the samples, and then scales and offsets the sum. The summation means that the Central Limit Theorem applies. The theorem states that the distribution of the sum of N random variables, taken from an arbitrary distribution, approaches a normal distribution as N increases.

For uniformly distributed random variables in the range [0,1], summing N=20 samples usually suffices for an engineering approximation of a normal distribution. Offsetting and scaling the sum are necessary because, although the distribution of the sum is approximately normal, the sum may not have the mean and variance desired for your application.

To transform the approximately normal sum's distribution into your desired normal curve, you must find the mean, $\mu$, and standard deviation, $\sigma$. Finding the mean and standard deviation using a closed-form solution is very difficult. Fortunately, useful approximations apply.

Because the algorithm uses only N samples from the uniform [0,1] distribution, the sum's mean is obviously N/2. Also the probability of generating a sum outside the range of [0,N] is exactly zero. So, to determine the standard deviation of the approximately normal sum's distribution, the algorithm equates the maximum possible value of the sum of N samples to the $6\sigma+\mu$, or "six sigma," point on the normal curve. This approximation yields a standard deviation of $\sigma=(N-\mu)/6$, which reduces to $\sigma=N/12$.

This approximation is valid because the probability of a datum occurring outside the $[-6\sigma-\mu,6\sigma+\mu]$ range is less than 1 in 500 million. For all practical purposes, 1 in 500 million is zero.

Next, assuming that the desired mean, $\mu'$, and standard deviation, $\sigma'$, differ from those of the N-sample sums' mean and deviation, transforming the sums takes three steps:

- First, shift the sum by subtracting N/2. This subtraction centers the N-sample sum's distribution at zero.
- Then, scale the upper and lower limits of the zero-centered distribution so that $N/2=6\sigma'$; that is, multiply the offset sum by $12\sigma'/N$.
- Finally, obtain the desired center value, $\sigma'$, by adding it as an offset.

The following equation succinctly expresses the algorithm:

$$z=\frac{12\sigma'}{N}\left(\sum_{i=1}^{N}x_i-\frac{N}{2}\right)+\mu'$$

where z is the approximately normal random variable with mean, $\mu'$, and standard deviation $\sigma'$ and $x_i$, from i=1 to N, are the samples.

You can easily encode this algorithm as a function in any programming language. The ZIPfile attached to **EDN BBS /DI_SIG #1690** contains a copy of this write-up. (DI #1690)

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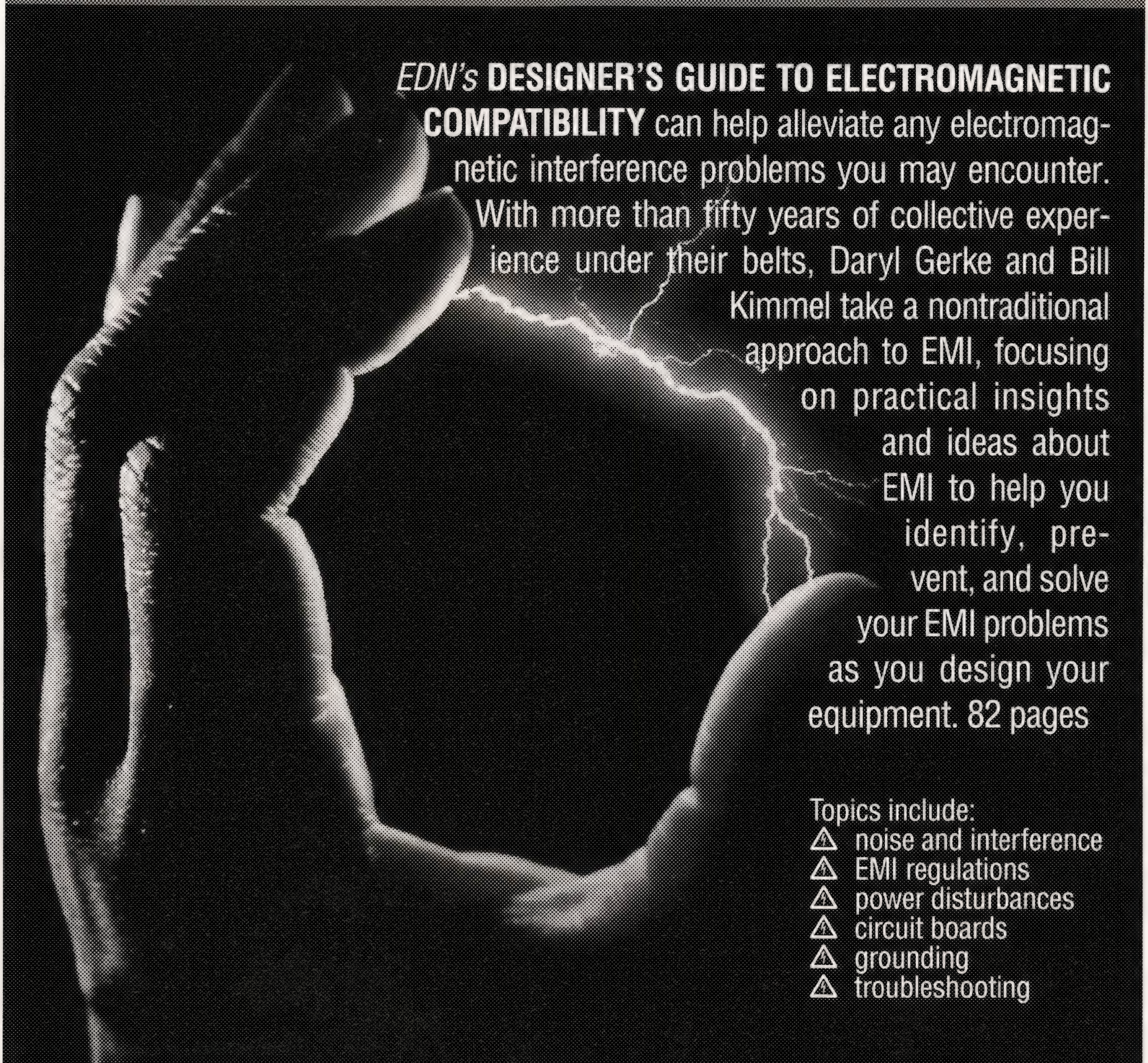
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# Two cores marry, make swinging choke

*VINCENT SPATARO, GEC MARCONI ELECTRONIC SYSTEMS CORP, WAYNE, NJ*

Designing an output choke for a switch-mode power supply that must operate over large load variations can be problematic. If you design the inductor for the maximum load the power converter will see, the inductance will be below the critical inductance required at light load. This inadequate inductance will cause the voltage on the output capacitor to peak up, resulting in increased ripple on the output.

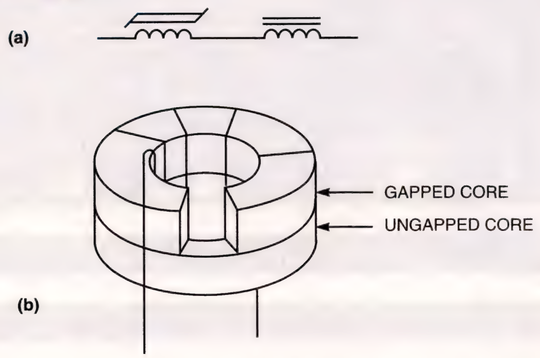
If, on the other hand, you design for the much larger value of inductance required at light load, your inductor will be overspecified for the nominal load and will be too large physically.

One solution is to add a bleeder resistor on the output of the supply to keep a minimum amount of current flowing at all times. This "fix" is not very efficient and often is an unacceptable solution, especially for battery-powered circuits.

A better solution is to use a swinging choke, which exhibits a large inductance at light load and a progressively smaller inductance as the load increases. The size of the swinging choke is considerably smaller than an overspecified conventional choke. And a swinging choke is more efficient than a bleeder resistor.

A new series of gapped ferrite toroids from Ferrite Specialties Inc (Conshohocken, PA) makes swinging-choke-design easy. You wind together a gapped ferrite toroid and an ungapped ferrite having the same form factor. The ungapped ferrite provides high inductance at light load but saturates at less than full load current. The gapped ferrite core provides much lower inductance at light load but doesn't saturate, providing a working inductance at full load. The result of the series combination of the two inductors is a single compact structure that doesn't require a coil bobbin and is easy to construct and mount. **Fig 1a** offers a schematic representation of the swinging choke; **Fig 1b** shows the mechanical construction.

**FIGURE 1**



**Winding an ungapped core together with a gapped core (a) forms a swinging choke (b) having ideal properties for the output choke of a switching power supply.**

As a design example, assume you want a 12.5-μH choke that operates at a nominal load current of 2A. This specification requires 20 turns of #18 AWG wire on a gapped Ferrite Specialties PGTX221406A36 core. This core has a gap $l_G$=0.0138 cm, a cross-sectional area $A_E$=0.259 cm, and an $A_L$=36 mH/1000T. At the nominal operating current of 2A, this core sees a flux density of

$$B=\left[\frac{0.4\pi LI^2}{A_E l_G}10^8\right]^{\frac{1}{2}}=1.32\ \text{kG}.$$

At this value for flux density, the core is operating far from saturation at nominal current and has plenty of design margin.

To design the high-inductance portion of the choke for the lightly loaded condition, use a standard ungapped ferrite core, a Philips 846T250-3C85. This core has an $A_L$=1220, μ=2000, and a magnetic path length $l_C$=5.42 cm. For the same number of turns, N, the inductance of this core is

$$L(\mu H)=\frac{N^2 A_L}{10^3}=488\ \mu H.$$

This core fully saturates at approximately B=5 kG. The current at this flux density is

$$I=\frac{Bl_C}{0.4\pi\mu N}=0.54A.$$

The total inductance of the core is the series combination of the gapped and ungapped inductors. At low current, the ungapped core dominates, producing a very large inductance. At 0.54A, however, the ungapped core saturates, reducing its inductance (essentially) to zero. The ungapped core then dominates, producing a working inductance at the full load current of 2A. The ZIP file attached to **EDN BBS /DI_SIG #1692** contains a copy of this write-up. (DI #1692)

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# CUT RS-232 NOTEBOOK SERIAL PORT SUPPLY CURRENT TO 1µA AND IMPROVE PERFORMANCE!

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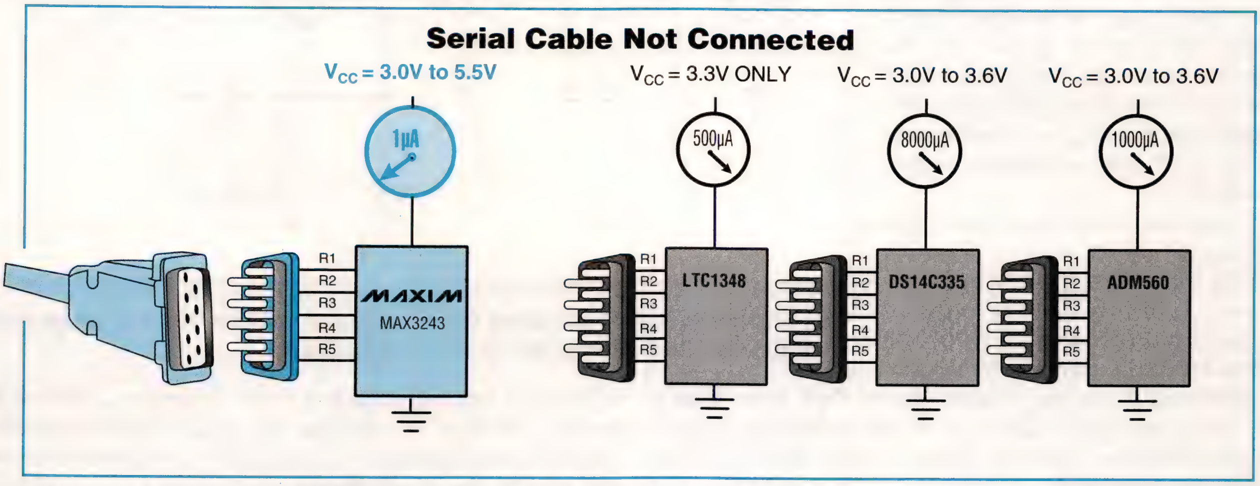

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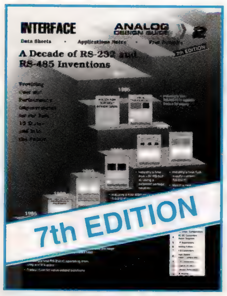
| LTC1348 | 3/5 | 500 | **3.3 only** | Yes | 5 x 0.1µF | No | 20 |
| DS14C335 | 3/5 | 8000 | 3.0 to 3.6 | Yes | 5 x 1.0µF | No | 20 |
| ADM560 | 4/5 | 1000 | 3.0 to 3.6 | No | 4 x 1.0µF | No | 20 |



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**North American inquiries, Circle No. 154 European inquiries, Circle No. 155**

# Spice model simulates broadband transformer

MICHAEL STEFFES, COMLINEAR CORP, FORT COLLINS, CO

The approximate model in Fig 1 makes it easier to include high-frequency transformers in a Spice simulation. Broadband pulse transformers are widely used to transform impedance levels as a noise-reduction or source-matching technique. **Fig 1** includes the physical model and the key performance equations. The model shows the transformer providing a voltage gain from $V_S$ to $V_O$, an input impedance of $R_L/n^2$, and an output impedance of $n^2R_S$.

To simulate the transformer, the Spice simulation requires $L_1$, $L_2$, and k as inputs. However, transformer manufacturers typically specify only an impedance ratio ($n^2$) and the two –3-dB frequencies of the transformer's bandpass response. If the passband is greater than two decades wide, which translates into k>0.98, the following Laplace bandpass transfer function approximates the frequency response for the model:

$$\frac{V_O}{V_S} \approx \frac{s\dfrac{R_{L/n}}{(1-k^2)L_1}}{\left(s+\dfrac{R_S+R_{L/n^2}}{(1-k^2)L_1}\right)\left(s+\dfrac{R_S\|\left(R_{L/n^2}\right)}{k^2L_1}\right)}, \qquad (1)$$

where the left denominator term determines the low-frequency cutoff of $2\pi f_L$ and the right denominator term determines the high-frequency cutoff of $2\pi f_H$. Manufacturers usually specify the –3-dB frequencies, $f_L$ and $f_H$, of broadband pulse transformers with $R_S$=50Ω and $R_L$=$n^2R_S$. You can solve **Eq 1** for the three required Spice model parameters as follows:

$$L_1=\frac{R_S/2}{2\pi f_L}=\frac{\dfrac{R_L}{2}\dfrac{1}{n^2}}{2\pi f_L}\,\Big|R_S=50\Omega,\ R_L=R_Sn^2$$

$$L_2=n^2L_1=\frac{R_L/2}{2\pi f_L}\,\Big|R_S=50\Omega,\ R_L=R_Sn^2$$

$$k=\sqrt{\frac{1}{1+4\dfrac{f_L}{f_H}}}.$$

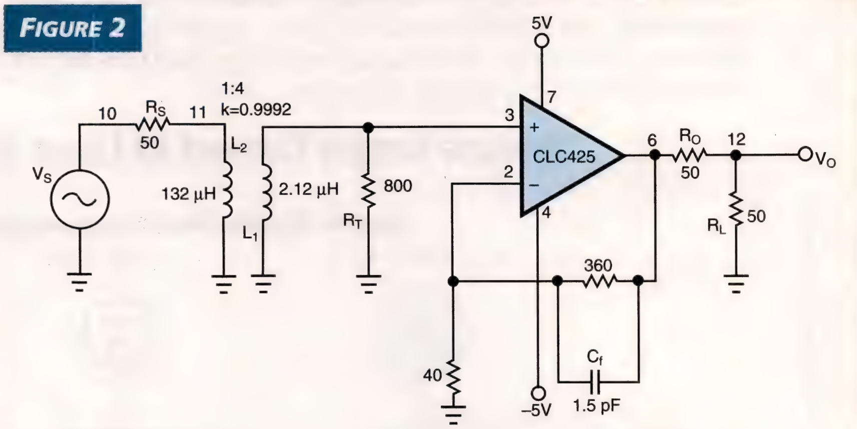
To illustrate how this model works, consider using a 1:4 transformer in front of a low-noise op amp to reduce its noise figure. The specifications for an RF Prime (Sacramento, CA, (916) 368-4400)) RFTM-16 transformer indicate an impedance ratio of 16 (n=4) and –3-dB frequencies of 30 kHz and 75 MHz. The three input parameters are as follows:

$$L_1=\frac{25\Omega}{2\pi(30\text{ kHz})}=132\ \mu H$$

$$L_2=\frac{400\,\Omega}{2\pi(30\,\text{kHz})}=2.12\ \text{mH}$$

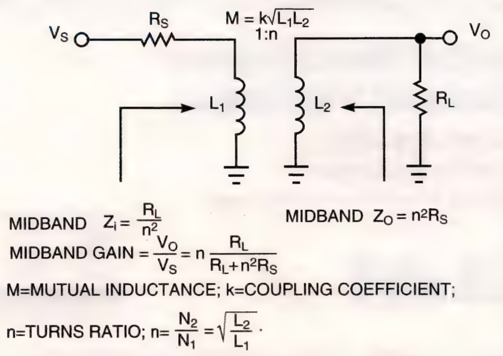
$$k=\sqrt{\frac{1}{1+4\left(\dfrac{30\text{ kHz}}{75\text{ MHz}}\right)}}=0.9992.$$

FIGURE 2



**This simulation test circuit places the transformer model in front of an op amp, a configuration that reduces the op amp's noise figure.**

FIGURE 1


$V_S$
$R_S$
$M=k\sqrt{L_1L_2}$
1:n
$V_O$
$L_1$
$L_2$
$R_L$
MIDBAND $Z_I=\frac{R_L}{n^2}$
MIDBAND $Z_O=n^2R_S$
MIDBAND GAIN $=\frac{V_O}{V_S}=n\frac{R_L}{R_L+n^2R_S}$
M=MUTUAL INDUCTANCE; k=COUPLING COEFFICIENT;
n=TURNS RATIO; $n=\frac{N_2}{N_1}=\sqrt{\frac{L_2}{L_1}}$.

**Using this approximate model of a high-frequency transformer, you can easily include transformers in a Spice simulation.**

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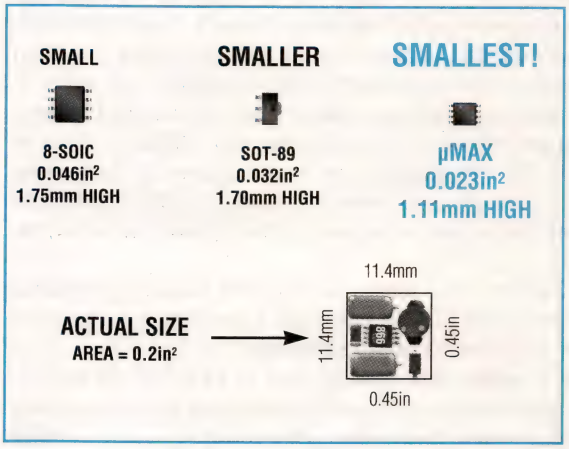

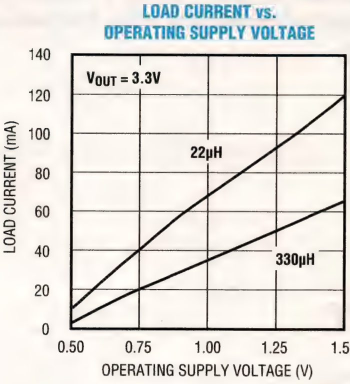

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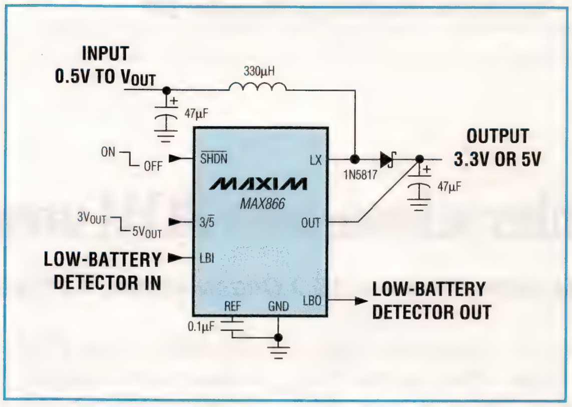

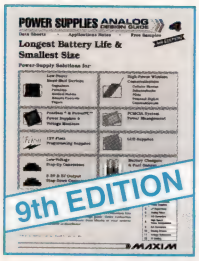
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You can now use the transformer model along with the op amp's macromodel to develop a full simulation for the test circuit in **Fig 2**. This circuit provides a good 50Ω input- and output-impedance match, a midband gain of +10 (20 dB) from the source to the matched load, and an input-noise figure that has been reduced from 9.5 dB for just the op amp to 4.2 dB with the input transformer.

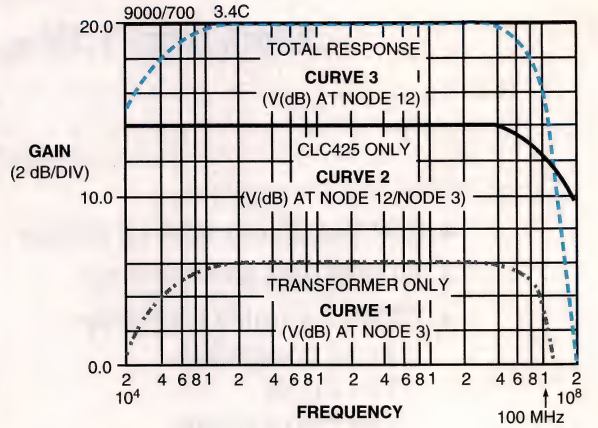
Curve 1 in **Fig 3** shows the response of the transformer only. With $R_T=n^2R_S$, the circuit attenuates $V_S$ by one-half to the input of the transformer and then provides a gain of n to the secondary side. The result is a net gain of +2 from the source to the input of the op amp. Curve 1 shows this midband gain and the correct low-frequency cutoff and also what appears to be second-order high-frequency roll-off. The op amp's input capacitance causes this roll-off, and removing the op amp shows exactly the desired 75-MHz single-pole roll-off for the transformer by itself. Curve 2 shows the response of the op amp alone. $C_F$ intentionally bandlimits the op amp's response to reduce high-frequency noise at the output.

Curve 3 is the total response from the source to the load showing the desired 20-dB gain with approximately the same frequency response as the transformer.

*Ed Note: The author thanks Paul Clark at RF Prime for his suggestion in applying high-frequency transformers and for verifying the simplified model shown here.* (DI #1681)

**To Vote For This Design, Circle No. 327**

**FIGURE 3**



**Three simulated curves of the transformer's response (Curve 1), the op amp's response (Curve 2), and the total response (Curve 3) confirm that this model produces the desired 20-dB gain with approximately the same frequency response as the transformer.**

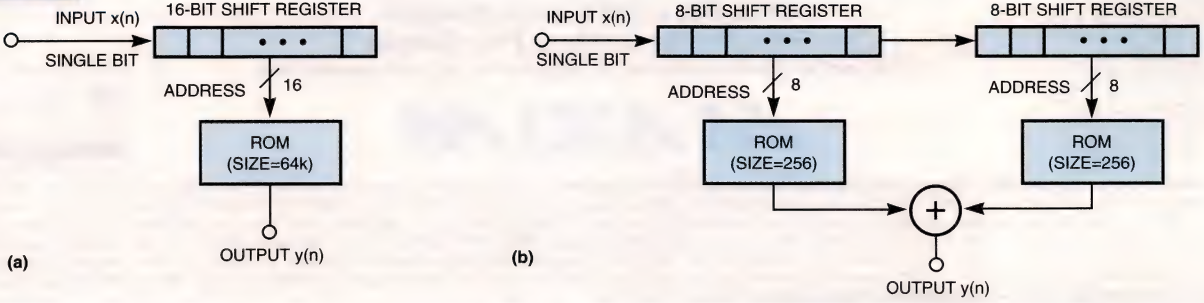
# FIR-filter scheme saves ROM storage space

*CA JALALUDEEN, DEFENCE R&D ORGANISATION, KOCHI, KERALA, INDIA*

You can easily implement single-bit FIR filters using ROM look-up tables, which allows you to avoid costly multiplier accumulators. Unfortunately, as filter order increases, so does the size of the ROM. **Fig 1** shows how you can reduce the storage requirement for larger-order filters.

The following difference equation defines an N-tap FIR fil-

**FIGURE 1**



**The direct implementation of an single-bit input FIR filter (a) requires a huge ROM as filter order increases. Splitting the summation in two or more partial sums (b) reduces ROM's storage requirements.**

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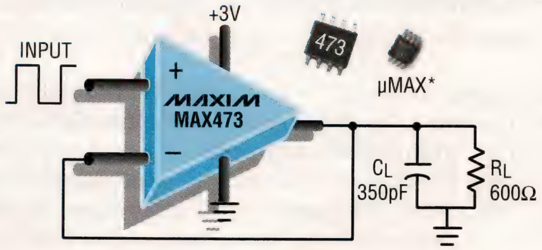

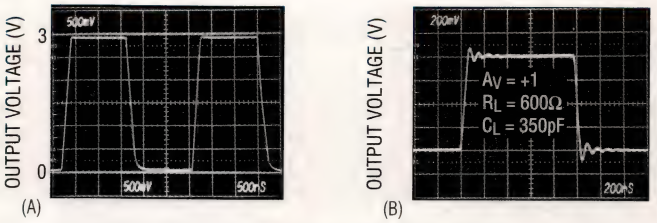

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ter, where y(n), x(n–m), and h(m) are, respectively, the output sequence, the input sequence delayed by m samples, and the impulse response (coefficients) of the filter:

$$y(h) = \sum_{m=o}^{N-1} h(m) \bullet x(n-m)$$

As the equation indicates, N multiplications and N–1 additions are necessary to calculate one sample of y(n). The direct implementation of the single-bit-input look-up-table approach simply uses a delay line (a serial-in, parallel-out shift register) and a ROM that stores all possible values of y(n) (**Fig 1a**). Although the input is a single bit, the output can be of any word length, depending on the word length of the filter coefficients.

When the order of the filter, N, becomes large, the size of the ROM becomes exorbitant. Fortunately, you can split the summation into two or more partial sums of smaller lengths as follows:

$$y(n) = \sum_{m=o}^{\frac{N}{2}-1} h(m) \bullet x(n-m) + \sum_{m=\frac{N}{2}}^{N-1} h(m) \bullet x(n-m)$$

**Fig 1b** shows a suggested implementation for a 16th-order filter based on this equation. This implementation requires only 512 locations of ROM compared with $2^{16}$=64k for the direct implementation. **Fig 1b** uses separate ROMs to store each sum and adds the partial sums together at the ROM outputs.

**Fig 2** shows an actual circuit implementation. The circuit latches the two 2716 ROM outputs using two 74LS374s for pipelining. Pipelining maximizes the speed of operation by splitting the ROM access time and the addition time of the adder. This circuit can operate with a sampling frequency equal to 1/T, where T is the access time of the ROM or the addition time of the adder, whichever is larger. The ZIPfile attached to **EDN BBS /DI_SIG #1689** contains this write-up and **figures** (in AutoCAD format). You can also easily extend the circuit for any order N. (DI #1689)

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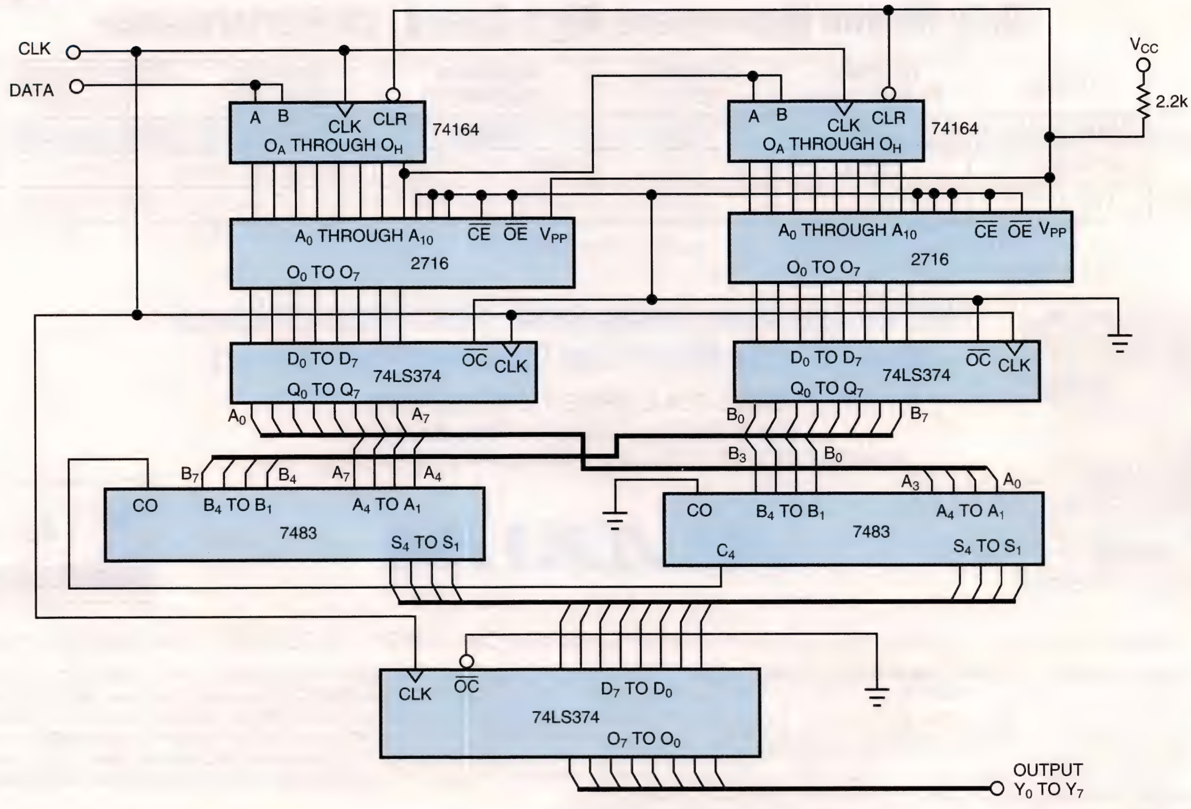
**FIGURE 2**



**This 16-bit FIR-filter circuit requires only 512 locations in ROM compared with the direct implementation's 64,000 locations.**

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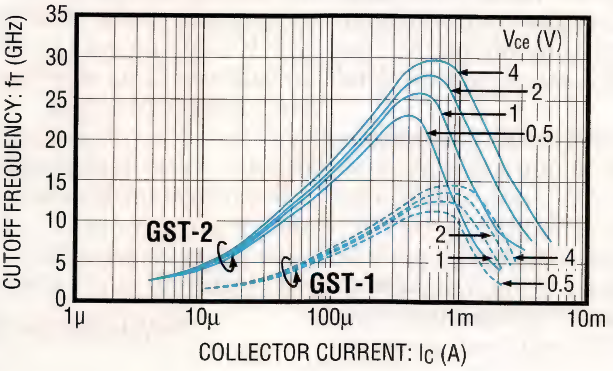

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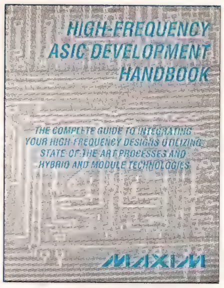
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- **UHF Local Oscillator**
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- **Power-Amp Driver**
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- **900MHz Upconverter**
- **IF Amplifier**
- **Power Control Block**

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# Sync separator includes AGC

**DANA ROMERO, SALT LAKE CITY, UT**

Proper sync separation in video-signal processing requires that the incoming signal be relatively stable. When substantial amplitude variation exists, a pair of ICs (**Fig 1**) combine to form a gain-control circuit that helps to stabilize the sync-separation function. $IC_1$ is a sync separator that has the features of the standard LM1881, plus horizontal sync decoding and a LEVEL-OUT pin to indicate the overall signal level at the input. Using this feature to control $IC_2$'s variable-gain amplifier, the circuit provides automatic gain control for sync separation. Most of the components surrounding $IC_1$ are close to the manufacturer's suggested values, and the data sheet explains their functions.

$IC_3$, a single-supply op amp, is the only other IC needed to complete the circuit. A single-supply op amp guarantees that the gain-control voltage at $IC_2$ remains positive while also performing the necessary translation of the LEVEL-OUT voltage from $IC_1$. Specifically, the dc voltage from $IC_1$'s pin 9 is nominally equal to twice the amplitude of the sync pulse of the video signal at pin 4. But, the negative feedback the entire loop requires means that the gain of $IC_2$ has to increase as the amplitude at $IC_1$'s pin 4 decreases. Connecting $IC_3$ as **Fig 1** shows accomplishes this function by inverting only the voltage changes from $IC_1$. $IC_3$'s overall output remains positive. In addition, potentiometer $R_1$ provides some auxiliary gain control. Note that a video-speed amplifier is not required for $IC_3$ because the overall level doesn't change at that rate.

$IC_2$ serves as a preamplifier for $IC_1$, and you must choose the feedback divider resistors, $R_2$ and $R_3$, so that their parallel resistance is low. (The data sheet for the EL4451 recommends a resistance of 360Ω or less.) Potentiometer $R_4$ sets $V_{REF}$ and adjusts the dc offset of the video signal out of pin 14. The equation for $V_{OUT}$ is

$$V_{OUT}=(V_{IN}\times V_G+V_{REF})/H,$$

where $V_{IN}$ is the voltage difference between pins 4 and 5, $V_G$ is the voltage difference between pins 7 and 8 (all pins of $IC_2$), and H is the feedback ratio $R_3/(R_2+R_3)$. Although $IC_2$ is designed to accept differential inputs for $V_{IN}$ and $V_G$, this design grounds pins 5 and 8. (DI #1700)

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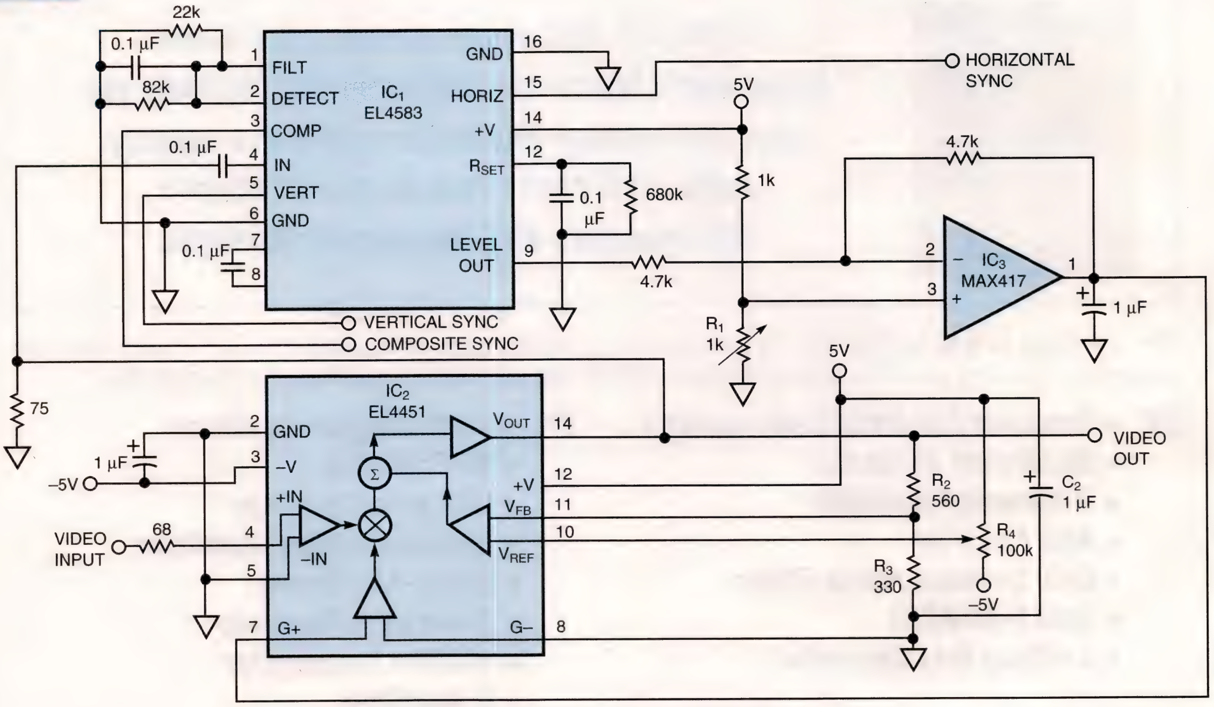
*(Design Ideas continued on pg 144)*

**FIGURE 1**



**A sync separator ($IC_1$), variable-gain amplifier ($IC_2$), and single-supply op amp ($IC_3$) form a gain-control circuit that helps to stabilize the sync-separation function.**

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DESIGN NOTES

# New LTC1266 Switching Regulator Provides High Efficiency at 10A Loads – Design Note 103

Greg Dittmer

The new LTC®1266 is a synchronous, step-down switching regulator controller that can drive two external, N-channel MOSFET switches. The superior performance of N-channel MOSFETs enables the LTC1266 to achieve high efficiency at loads of 10A or more with few additional components. Burst Mode™ operation provides high efficiency at light loads—efficiency is greater than 90% for loads from 10mA to 10A. The ability to provide 10A at high efficiency is critical for supplying power to Pentium™ processor applications.

The LTC1266 is based on the LTC1148 architecture and has most of the features of this successful product including constant off-time, current mode architecture with automatic Burst Mode operation. Pin selectable shutdown reduces the DC supply current to 40μA. The LTC1266 also provides pin selectable phase of the top-side driver which allows it to implement, in addition to an all N-channel step-down regulator, a low dropout regulator with high-side P-channel or a boost regulator. Other new features of the LTC1266 include an on-chip low-battery comparator, pin-defeatable Burst Mode operation, a wider voltage supply range (3.5V to 20V), 1% load regulation and a higher maximum frequency of 400kHz.

## N-Channel vs P-Channel

The key to the LTC1266's ability to drive large loads at high efficiencies is its ability to drive both top-side and bottom-side N-channel MOSFETs. The superiority of N-channel MOSFETs over P-channels at high currents is due to the lower $R_{DS(ON)}$ and lower gate capacitance of the N-channel parts. To compensate for the higher $R_{DS(ON)}$, the P-channel size is usually made larger, resulting in higher gate capacitance. Efficiency is inversely proportional to both $R_{DS(ON)}$ and gate capacitance. Higher $R_{DS(ON)}$ decreases efficiency due to higher $I^2R$ losses and limits the maximum current the MOSFET can handle without exceeding thermal limitations. Higher gate capacitance increases losses due to the increased charge required to switch the MOSFETs on and off during each switching cycle.

Nonetheless, P-channel MOSFETs still have a home in lower current and low dropout applications due to the fact they can operate at 100% duty cycle. The LTC1266 offers the capability of driving either N-channel or P-channel.

## Driving N-Channel MOSFETs

P-channels have another distinct advantage—simplicity of the gate drive. Because of the negative threshold of the P-channel, the gate potential must decrease below the source (which is at $V_{IN}$) by at least $V_{GS(ON)}$ to turn it on. Hence, the top-side MOSFET can be gated between the available supply rail $V_{IN}$ and ground.

Driving an N-channel top-side MOSFET isn't so straightforward. When the top-side MOSFET is turned on, the source is pulled up to $V_{IN}$. Because the N-channel has a positive threshold voltage, the gate must be above the source by at least $V_{GS(ON)}$. Thus, the top-side drive must swing between ground and $V_{IN} + V_{GS(ON)}$. This requires a second, higher supply rail equal to at least $V_{IN} + V_{GS(ON)}$.

There are two ways to obtain this higher rail. The most straightforward way is to use a higher rail that is already available, as is the case in most desktop systems with 12V supplies. Note that the PWR $V_{IN}$ input to the LTC1266 is dedicated to powering the internal drivers and is separate from the main supply input. The PWR $V_{IN}$ voltage cannot exceed 18V (20V max), limiting the input voltage to 18V – $V_{GS(ON)}$. For a converter with logic-level MOSFETs, this limits $V_{IN}$ to about 13.5V. The PWR $V_{IN}$ voltage must also meet its minimum requirement of $V_{IN} + V_{GS(ON)}$ (about 10V for a 5V-to-3.3V converter) in order not to burn up the high-side MOSFET due to insufficient conductance at larger output loads. If a higher supply rail is not available, a charge-pump circuit can be used to pump $V_{IN}$ to the required level.

---

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## Basic Circuit Configurations

Figures 1 and 2 show two basic circuit configurations for the LTC1266. Figure 1 shows an LTC1266 in the charge pump configuration designed to provide a 3.3V/10A output. The Si4410s are new logic-level, surface mount N-channel MOSFETs from Siliconix that provide a mere 0.02Ω of on-resistance at $V_{GS}$ = 4.5V, and thus provide a 10A solution with minimal components. The efficiency plot shows that the converter still is close to 90% efficient at 10A. Because the charge pump configuration is used, PWR $V_{IN}$ = 2 × $V_{IN}$ plus any additional ringing on the switch node. Due to the high AC currents in this circuit, we recommend low ESR OS-CON or AVX input/output capacitors to maintain efficiency and stability.

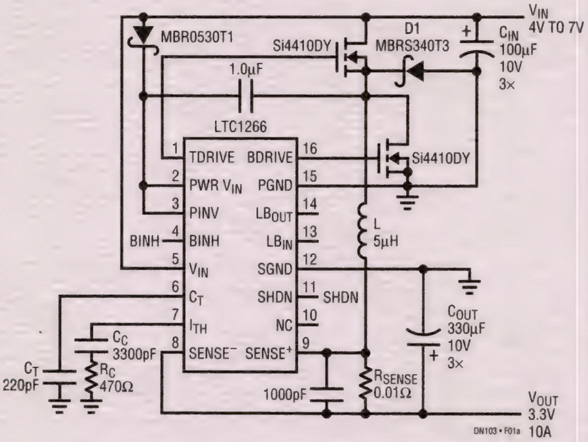

**Figure 1a. All N-Channel Single Supply 5V to 3.3V/10A Regulator**

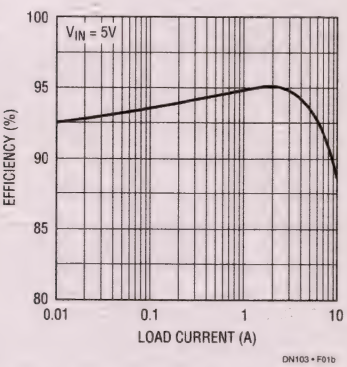

**Figure 1b. Figure 1a Circuit Efficiency**

The all N-channel, external PWR $V_{IN}$ circuit shown in Figure 2 is a 3.3V/5A surface mount converter. The current sense resistor value is chosen to set the maximum current to 5A, according to the formula $I_{OUT}$ = 100mV/$R_{SENSE}$. With $V_{IN}$ = 5V, the 5µH inductor and 130pF timing capacitor provide an operating frequency of 175kHz and a ripple current of 1.25A. The $V_{GS(ON)}$ of the Si9410 N-channel MOSFETs is 4.5V; thus the minimum allowable voltage at the external PWR $V_{IN}$ is $V_{IN(MAX)}$ + 4.5V. At the other end, PWR $V_{IN}$ should be kept under the maximum safe level of 18V, limiting $V_{IN}$ to 18V – 4.5V = 13.5V.

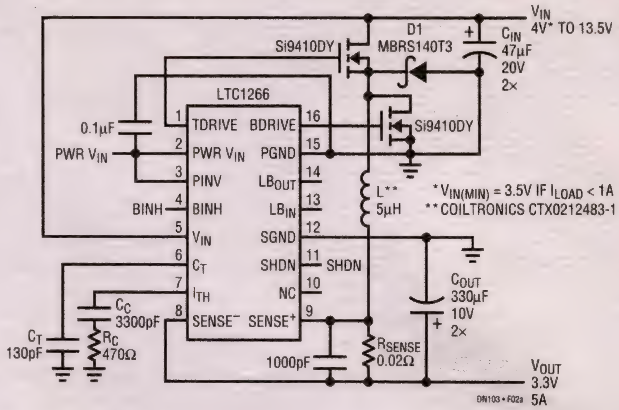

**Figure 2a. All N-Channel 3.3V/5A Regulator with Drivers Powered from External Power $V_{IN}$ Supply**

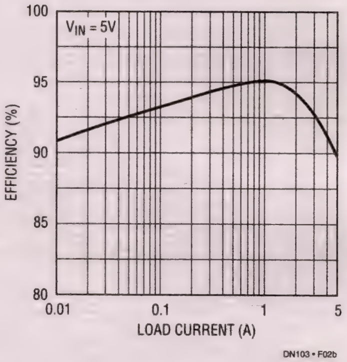

**Figure 2b. Figure 2a Circuit Efficiency**

The two application circuits demonstrate the fixed 3.3V version of the LTC1266. The LTC1266 is also available in fixed 5V and adjustable versions. All three versions are available in 16-pin narrow SOIC packages.

## Conclusion

The new LTC1266 synchronous step-down regulator controller is the first Linear Technology synchronous controller with the ability to exploit the superior performance of N-channel MOSFETs to maximize efficiency and provide a low cost, compact solution for high current converters. The extra features provided in this product, Burst Mode inhibit and a low-battery comparator, make it ideal in a wide variety of applications.

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***Test & Measurement***
**1990** - Crosscheck Test Technology, Crosscheck Technology Inc.
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**1992** - 90-Series Scopemeters, John Fluke Mfg Co Inc./Philips Test and Measurement
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# Single IC adds analog inputs to digital PLC

***Steve Hageman, Calex Manufacturing Co, Concord, CA***

Many low-cost programmable logic controllers (PLCs) are digital only and have relay outputs, debounced digital inputs, and one or more counter inputs. The circuit in **Fig 1** adds four 8-bit analog inputs to even the most basic PLC. The design requires a PLC with just two digital outputs and one high-speed (>5 kHz) counter input. The circuit is based on Microchip Technology's (Chandler, AZ) PIC 16C71 RISC μC. This μC has a four-channel, 8-bit ADC and an 8-bit digital I/O port. The digital I/O port has built-in pullup resistors, so direct interface to relays is possible.

The PIC operates by sensing a low-to-high change on the RB0 input. This change causes a wake-up interrupt in the PIC. After some suitable debounce interval (50 msec), the PIC selects A/D channel 0, 1, 2, or 3, depending on the address at RB0 and RB1. The PIC sets the channel, waits for the input multiplexer to settle, and reads the ADC's result. The PIC has converted the analog input to a 0-to-255 digital byte.

The PLC's counter input now helps transfer this digital value into the PLC. The PIC shifts out the digital code as a string of pulses at 5 kHz. The pulse train is 0 to 255 counts long, depending on the value of the sampled A/D channel. The following equation translates the digital count to a voltage:

$$\text{Voltage input}=\text{digital code}\times 0.0195.$$

So, if the PLC reads a value of 130 from the counter after a conversion, the voltage on that channel is 2.53V (130×0.0195).

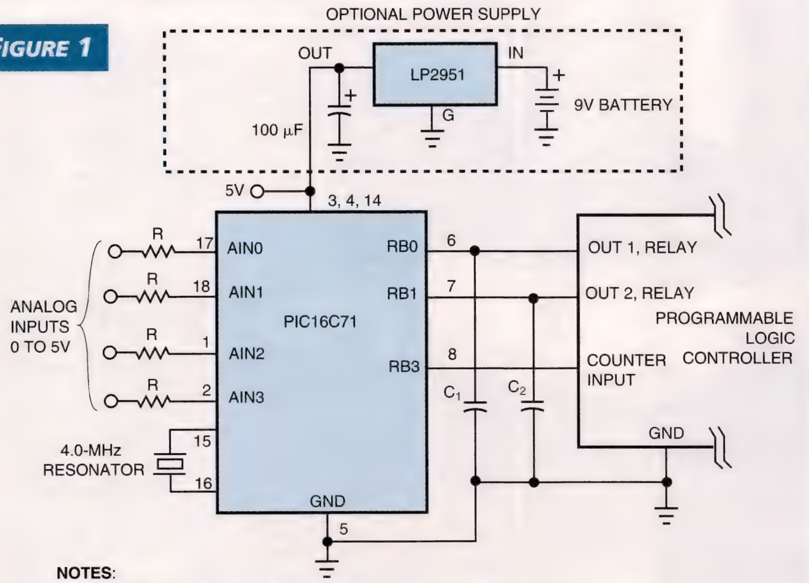
At a 5-kHz transfer rate, it may take up to 51 msec to completely transfer all 255 counts to the PLC's counter. After a complete transfer, the PIC waits for a low-to-high transition on the RB0 input pin to restart the process. **Fig 2** is a flow diagram of the PLC's program.

If a convenient 5V source isn't available for powering the PIC μC, you can drive the circuit using the optional power supply in the **Fig 2.** A 9V alkaline battery can continuously power the circuit for over 250 hours. Longer life is possible if you use a PLC-relay output to switch the power on and off. For long term, unattended operation, you can substitute a 9V wall-cube transformer from Radio Shack for the 9V battery.

The PIC was programmed in C, using a low-cost C compiler. Even using a high-level language such as C, this interface program consumes only about one-quarter of the PIC's 1-kbyte available program space. The ZIPfile attached to **EDN BBS /DI_SIG #1701** contains the HEX object file to program your own PIC, along with the C source code. (DI #1701)

**To Vote For This Design, Circle No. 330**

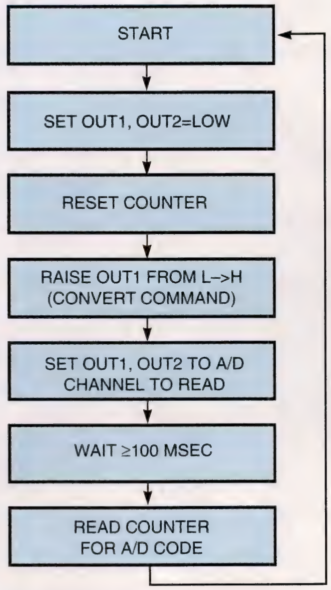
**FIGURE 1**



NOTES:
$C_1$, $C_2$ ARE 0.1 μF TYP FOR DEBOUNCE.
R<10k, TYPICALLY 4.7k FOR ESD PROTECTION.

**This circuit adds four 8-bit analog inputs to even the most basic PLC.**

**FIGURE 2**


START
SET OUT1, OUT2=LOW
RESET COUNTER
RAISE OUT1 FROM L->H (CONVERT COMMAND)
SET OUT1, OUT2 TO A/D CHANNEL TO READ
WAIT ≥100 MSEC
READ COUNTER FOR A/D CODE

**This PLC program interfaces with the PIC μC.**

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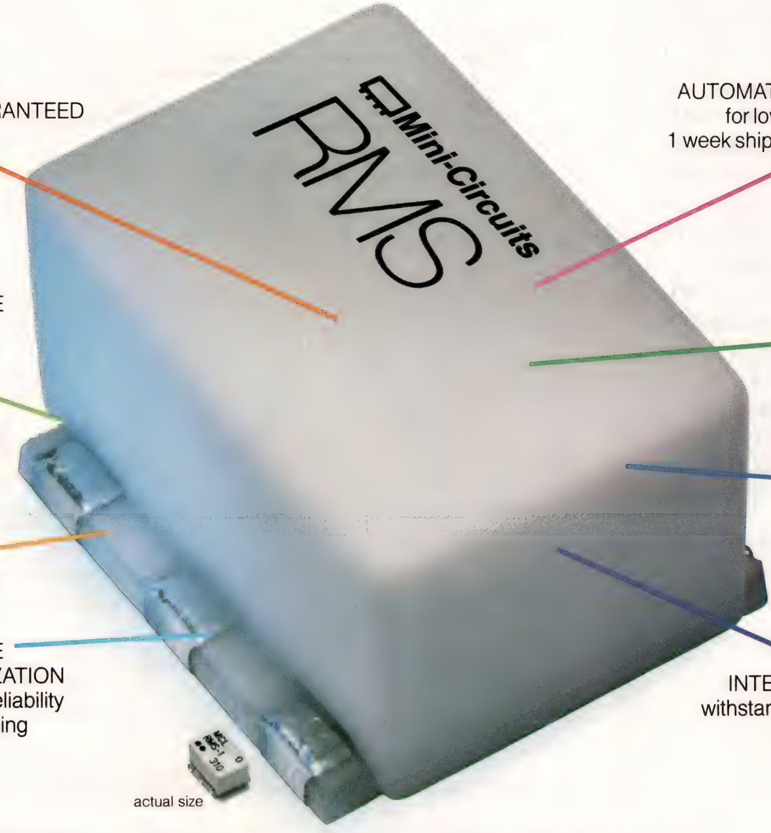

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CIRCLE NO. 202

# Synchronized window comparator eliminates error

***SERGEY VELICHKO, CONSULTANT, BOSIE, ID***

Precision A/D converters need a window comparator. The window comparator in **Fig 1a** is synchronized to the clock signal. This synchronization eliminates errors that could arise when the input signal crosses the high or low threshold (**Fig 1b**) unsynchronized to clock.

In operation, comparator $IC_{1A}$ sets flip-flop $IC_{2A}$ high when the input signal rises above the high threshold. Inverting comparator $IC_{1B}$ sets flip-flop $IC_{2A}$ low when the input signal descends past the low threshold. The second flip-flop, $IC_{2B}$, synchronizes the first flip-flop's output to the rising edge of the clock signal. Obviously, the clock signal must be significantly higher in frequency than the input signal to avoid problems with metastability.

The values for $R_2/R_3$ and $R_4/R_5$ determine the hysteresis for the comparators. Customary values for $R_2$ and $R_3$ are 10 kΩ and 1 MΩ for $R_4$ and $R_5$. Reference-voltage $V_1$, $R_1$, and $R_2$ determine this high threshold. Similarly, reference-voltage $V_2$, $R_6$, and $R_7$ set the low threshold. (DI #1693) EDN

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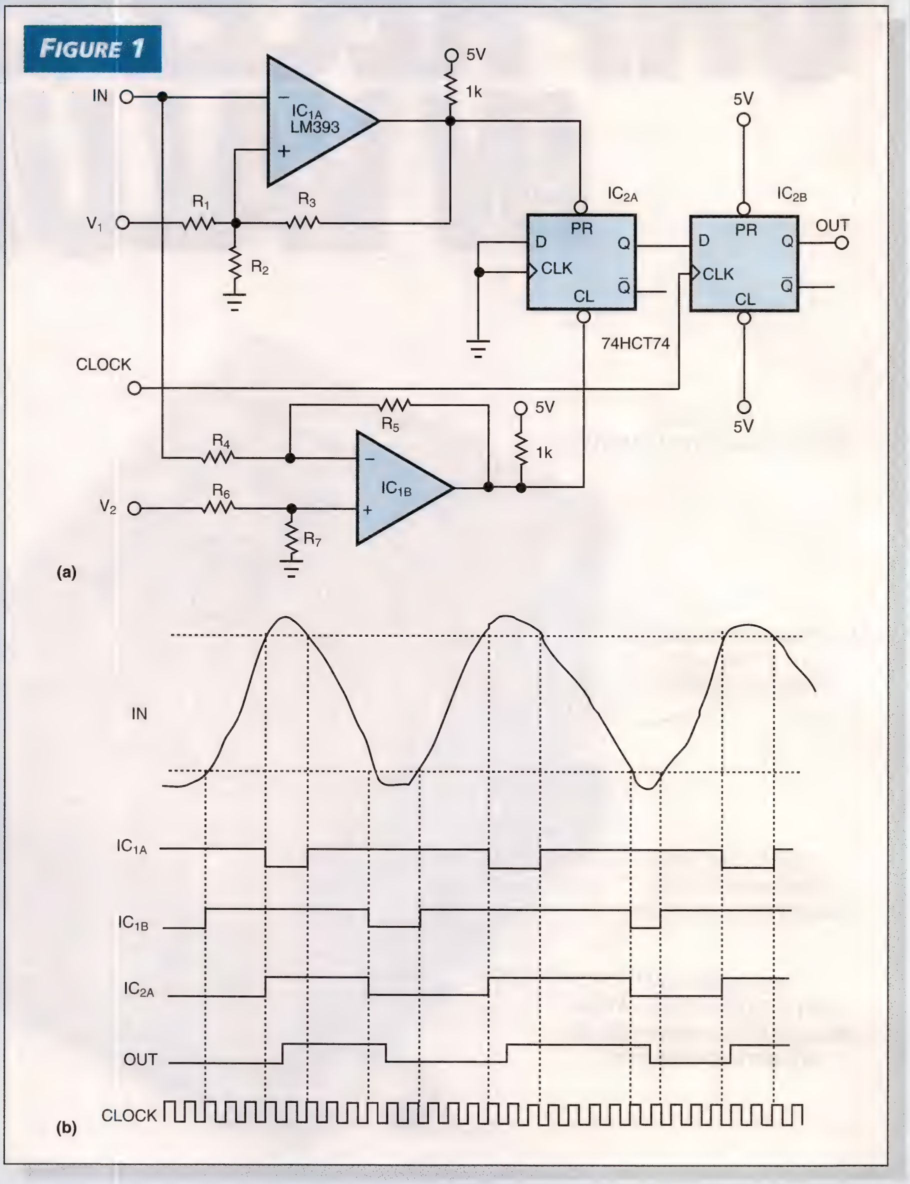
**FIGURE 1**



**The output of this window comparator is synchronous with the clock signal.**

---

# Token passing fits large counters into CPLDs

***CHRIS JONES AND DAVID JOHNSON, CYPRESS SEMICONDUCTOR CORP, SAN JOSE, CA***

Fitting a large, loadable counter into a complex PLD (CPLD) while operating at the device's maximum frequency requires a few tricks. **Fig 1** shows a 40-bit, loadable counter with a terminal-count output. The problem with fitting this design into a CPLD is that the design exceeds the usual number of logic-block inputs, which is 36 or fewer. Normally, for the

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[1] Sample suite of GPIB programmed audio measurements included 1) noise measurement (20Hz-22kHz bandpass), 2) 31 point single tone frequency response sweep over 20Hz-22kHz range, and 3) 11 point distortion sweep over 20Hz-22kHz range.

[2] *FAST*TEST uses multi-tone stimulus and analysis to make the same measurements listed above.

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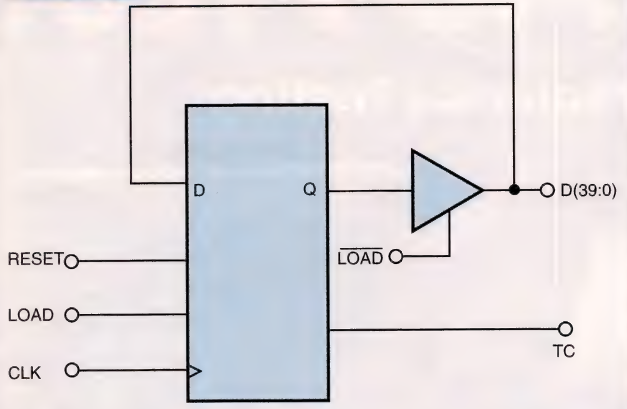
CIRCLE NO. 68

**FIGURE 1**



Fitting this 40-bit, loadable counter into a CPLD requires a few tricks because the design exceeds the usual number of logic-block inputs, which is 36 or fewer.

most significant bit of a 40-bit counter, you must route 43 inputs into the logic block that registers: the 40 counter bits, the load control, the asynchronous-reset input, and that bit's data input for loading.

This design demonstrates how you can use token passing to fit large, loadable counters within a CPLD's available number of logic-block inputs. Registering these tokens allows the resulting design to operate at the CPLD's maximum frequency. These tricks are the keys to the successful implementation of a large, loadable counter in a CPLD.

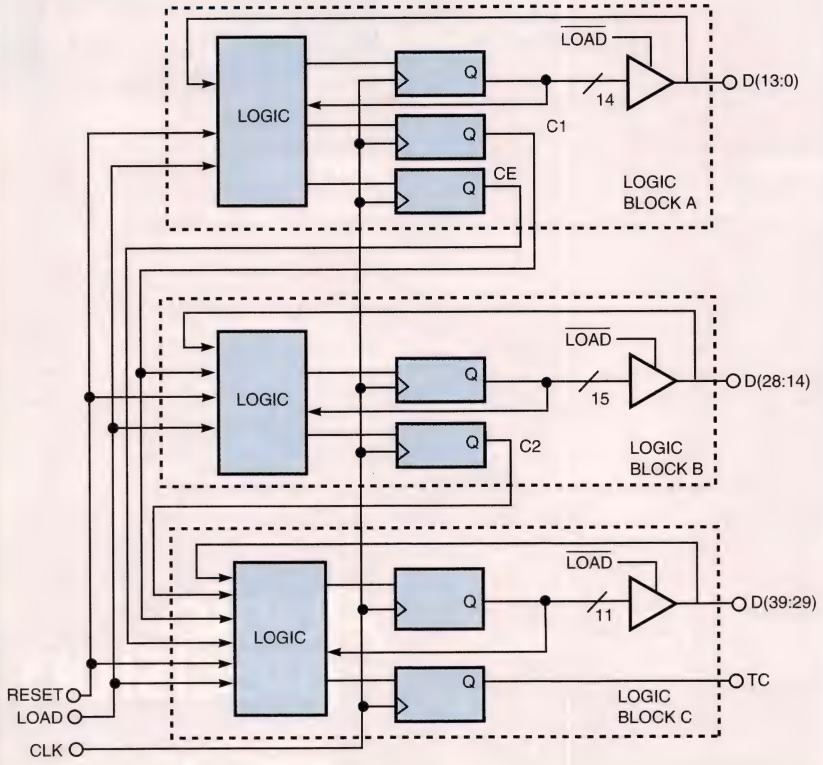
**Fig 2** shows how you can fit the counter into a 64-macrocell CPLD, the Flash370 CY7C373, while operating at full frequency. To ensure that the number of logic-block inputs is no more than 36, the design divides the counter into three groups. Two tokens in logic block A and one token in logic block B pass the necessary information regarding the state of the respective counter groups among counter groups. You must register the tokens for the resulting design to operate at the device's maximum frequency.

C1, C2, and CE operate as follows. C1 loads a 1 when the 14 counter bits in block A are all 1s. This setting of C1 can happen during a load operation or when the counter increments during normal counting. A C1 of 1 indicates that the 15 counter bits in block B need to increment on the next clock. Similarly, C2 loads a 1 when the 15 counter bits in block B are all 1s. The AND of C1 and C2 increments the enable for the 11 counter bits in block C. CE sets to a 1 when the 14 counter bits in block A are loaded with the HEX value of "3FFE." The states of CE, C2, and the 11 counter bits in block C determine when the terminal-count output, TC, becomes active.

We coded the design in VHDL. We compiled, synthesized, and targeted the design to the 64-macrocell CY7C373 using the Warp3 software-development system. The simulation shows that the TC output is active as desired when all 40 counter bits are 1. The TC output then changes to a 0 as the counter properly increments from all 1s to all 0s on the next clock. (DI #1702) EDN

**To Vote For This Design, Circle No. 332**

**FIGURE 2**



To fit this 40-bit counter into one CPLD (the Flash370 CY7373), this design divides the counter into three groups and uses tokens C1, C2, and CE to pass information among the groups.

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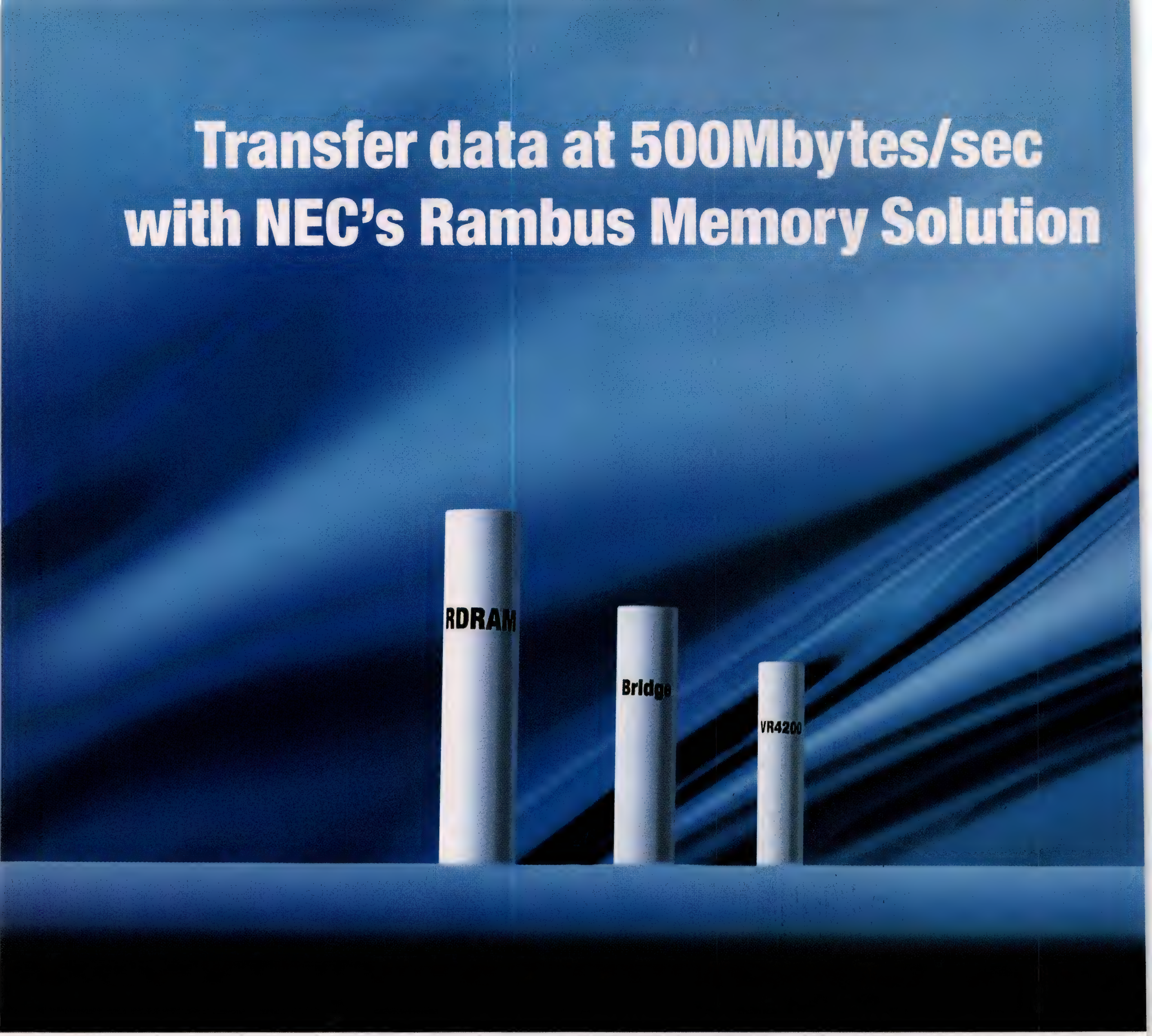
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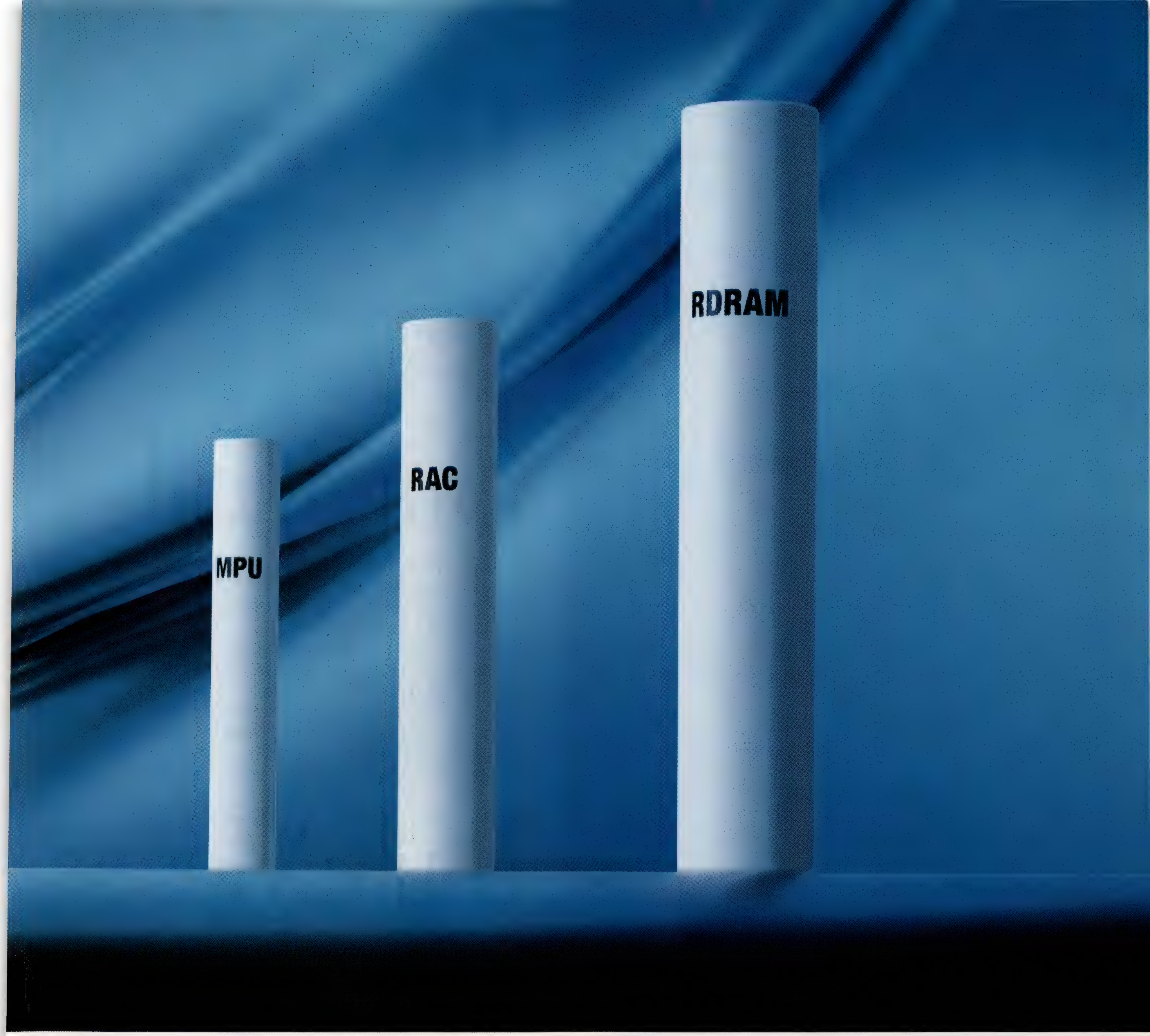

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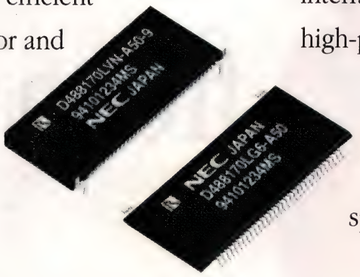

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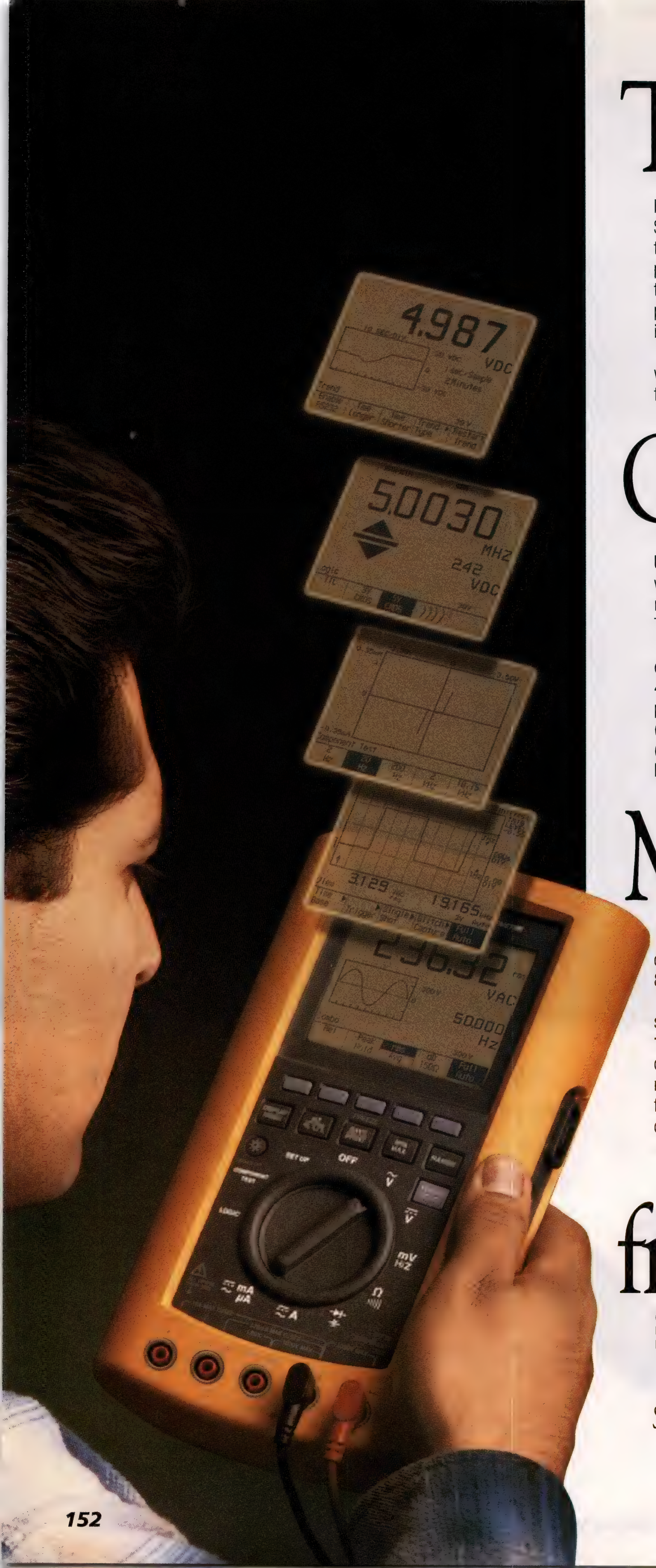

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CIRCLE NO. 149

# Detailed model shows FPGAs' true costs

### JOSEPH LIU, XILINX ASIA PACIFIC

Design decisions are far more complex than simply weighing the unit price and NRE charge to determine whether to use FPGAs or ASICs. An analysis of all the variables affecting IC development shows that FPGAs are extremely cost-effective at surprisingly high production volumes.

PLDs, particularly field-programmable gate arrays (FPGAs), have been gaining momentum over traditional ASICs as the logic device of choice for today's fewer than 20,000-gate system designs. A primary concern in choosing PLDs, however, is their suitability for high-volume production. Historically, because of their higher unit price, FPGAs have been considered appropriate for prototyping or low-volume production, while mask-programmed gate arrays have been viewed as more cost-effective for high-volume applications.

## The "cost-of-ownership" equation

Gate arrays and other mask-programmed ASICs have many hidden costs. Unit price and NRE charges become a small part of the cost when you consider the loss of flexibility and the increased time to market. By applying simple formulas to the specifications of a development program, you can easily examine the break-even points and total costs.

Among the factors that determine cost of ownership are:

- unit price
- NRE charges
- production leadtimes
- gate count
- tools
- time to volume
- future cost reductions
- technology
- test development
- flexibility
- volume package type
- design time
- re-spin potential
- expedite fees
- engineering time
- fault coverage
- quality
- vendor service
- inventory
- risk.

Some of these factors are interdependent. For example, lengthening production leadtime can affect inventory, time to volume, expediting fees, and risk. Also, many of these costs can go unrecognized in a traditional cost analysis, because they are incurred after the design is finished or because they cut across many functional groups, such as purchasing, engineering, and quality assurance.

The following analysis uses a typical 10,000-gate design to demonstrate how to find the break-even point and cost of ownership for an FPGA vs an ASIC. You can use the same formula for any application or situation.

FPGAs provide the benefits of standard products—no NRE charge, quick delivery, and no inventory risk—with fully tested components. In addition, users can verify a design in-circuit and make changes anytime. In comparison, although gate arrays or custom ASICs offer the lowest unit cost, they suffer from long, rigorous development cycles, with the risk and inflexibility of nonprogrammability.

Most factors that dramatically affect the cost of using an

**TABLE 1—FPGAs VS GATE ARRAYS**

| Programmable FPGA | Gate array |
|---|---|
| Standard product | Custom product |
| Off-the-shelf delivery | Months to manufacture |
| Fast time to market | Slow time to market |
| User programmable | Nonuser programmable |
| No NRE | NRE, expedite charges |
| No inventory risk | Customer specific |
| Fully factory tested | User test development |
| Simulation helpful | Simulation critical |
| In-circuit design | No in-circuit design |
| Verification | Verification |

ASIC are intangibles. Even though these costs don't show up on a purchase order, they are measurable and should be included in your design decision (**Table 1**).

**Table 2** lists attributes and costs you would need for determining the true costs of ASICs. By filling in the blanks with the costs for your project, you can tailor this analysis to your situation. The numbers in this sample analysis are "typical numbers," according to worldwide research by Dataquest and Integrated Circuits Engineering (ICE), two market research companies.

### TABLE 2—DETERMINING ASIC COSTS

| | | | |
|---|---|---|---|
| **Design attributes** | | | |
| 1 | Number of gates in the design | | 10,000 |
| 2 | Package type | | PQFP |
| 3 | Selling price of end system | | $2000 |
| 4 | Cost of end system | | $1100 |
| 5 | Product life in months | | 36 |
| 6 | Engineering $$ per person per week[1] | | $3000 |
| **Product forecast**<br>(total volume of this device used in the product) | | | |
| 7 | Year 1 | | 1000 units |
| 8 | Year 2 | | 12,000 units |
| 9 | Year 3 | | 5000 units |
| 10 | Year 4 | | — |
| 11 | Year 5 | | — |
| | **Attributes** | **ASIC** | **FPGA** |
| 12 | Engineering costs | $79,000 | $25,000 |
| 13 | NRE | $25,000 | $0 |
| 14 | tools | $10,000 | $10,000 |
| 15 | Average price | $13 | $39 |
| 16 | Engineering labor in weeks | — | 4 |
| 17 | Training in weeks | 2 | 1 |
| 18 | Design capture in weeks | 3 | 2 |
| 19 | Simulations in weeks | 2 | 2 |
| 20 | Test-vector development in weeks | 6 | 0 |
| 21 | Place and route in weeks | 1 | 1 |
| 22 | Back annotations/DRCs in weeks | 1 | 0 |
| 23 | Final simulations in weeks | 1 | 0 |
| 24 | Proto cycle time in weeks | 2 | 0 |
| 25 | Qualification in weeks | 5 | 3 |
| 26 | Production leadtime in weeks[2] | 9 | 2 |
| 27 | Potential for a re-spin expressed as a percentage of probability[3] | 30% | |

**Notes:**

[1] Industry standard is $3000.

[2] Industry average for gate arrays is eight to 14.

[3] Industry average is 12% due to manufacturer error and 20% due to customer design changes.

## Price*volume is deceiving

The evaluation of whether to use an FPGA or ASIC must include more than a basic price*volume analysis to realistically model true costs. Surprisingly, time to market, not unit price and NRE cost, has the greatest bearing on the cost of your design. To demonstrate, start with a basic break-even model and adjust it for time to market and other crucial factors.

The basic formula is:

$$\text{Basic break even} = \text{NRE}+\text{engineering}+(\text{units}*\text{price}) \quad (1)$$

Gate arrays or ASICs have a much higher development cost than do FPGAs. Because of higher component price, FPGAs have traditionally been used in lower volume applications. However, that trend has reversed itself. FPGAs have no NRE charges, and their design cycles are short. However, if you consider only the fixed costs of a stable design in choosing an implementation, an FPGA's low entry costs eventually converge with the unit price of an ASIC.

Using the typical data from **Table 2**:

$$\text{ASIC} = \$25{,}000\ \text{NRE}+\$79{,}000\ \text{engineering and tools}+(X\ \text{units}*\$13). \quad (2)$$

$$\text{FPGA} = 0\ \text{NRE}+\$25{,}000\ \text{engineering and tools}+(X\ \text{units}*\$39). \quad (3)$$

Solving for the break even:

$$X=79{,}000/26=3038\ \text{units}. \quad (4)$$

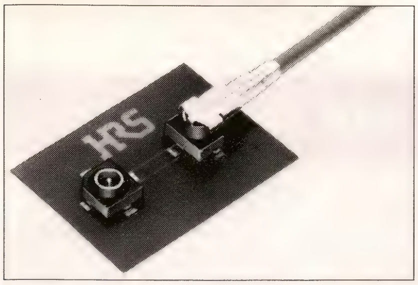
Using this equation, when you take into consideration only the fixed costs of NRE, engineering dollars, and unit price, the break-even point between a mask-programmed

### TABLE 3—COMPARATIVE DEVELOPMENT TIME

| Item | Stages | ASIC (weeks) | FPGA (weeks) |
|---|---|---|---|
| 17 | Training | 2 | 1 |
| 18 | Capture | 3 | 2 |
| 19 | Simulation | 2 | 2 |
| 20 | Test-vector development | 6 | 0 |
| 21 | Place and route | 1 | 1 |
| 22 | Back annotation | 1 | 0 |
| 23 | Final simulation | 1 | 0 |
| 24 | Proto cycle | 2 | 0 |
| 25 | Qualification | 5 | 3 |
| 26 | Production leadtime | 9 | 2 |
| Total time | | 32 | 11 |

ASIC=32 weeks – eight months to production
FPGA=11 weeks – 2.75 months to production

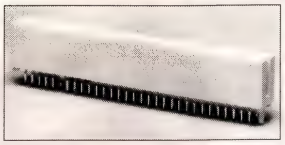
## WORLD'S SMALLEST SMT CO-AXIAL CONNECTOR



Hirose has introduced its H.FL series SMT low-profile super-miniature coax connector; at a mated height of only 3mm (plug plus board-mount receptacle), it's the world's smallest. The H.FL series offers plug to receptacle mating at 360-degree orientation; solderless crimping for connector top cable termination and a tool for unmating the plug and receptacle. The H.FL coax has high frequency characteristics of DC -3000 MHz/V.S.W.R. below 1.3, for up to 3 GHz. Applications include cellular telephones, radio communications equipment, GPS and other projects requiring small coaxial connectors. For further information, contact **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958 ask for extension 24 or 29. Fax (805) 522-3217.

**CIRCLE #36**

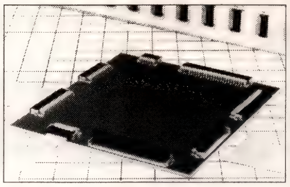
## HALF-PITCH CARD EDGE CONNECTOR FOR PCI BUS



Hirose is now providing the CR27, a half-pitch (1.27mm) card edge connector for PCI bus (Peripheral Component Interconnect). The high density CR27 features 120 contacts and can be used with either a 32-bit 5V or 3.3V specification. This is useful when designing for fast connecting of interface components to a computer or a wide variety of office automation products. The CR27 meets PCI Local Bus Specification 2.0. Contacts on the CR27 are preloaded to offer a stable contact. Positioning bosses and standoffs are provided for effective flux cleaning. **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958, ask for ext. 24 or 29. Fax (805) 522-3217.

**CIRCLE #37**

## 1MM SMT/ZIF-TYPE FLEXIBLE PCB CONNECTORS



Hirose has introduced a 1mm contact spacing connector to its FH12 series which features a new concept in "flip-lock" SMT/ZIF flexible printed circuit board connectors. The 1mm contact spacing is a half loaded version of the FH12 series of 0.5mm contact spacing connectors. These connectors are ideal for use with miniature FPC/FFC for SMT and avoid the problems associated with traditional slide lock systems. The flip lock latch allows these connectors to stack end to end. Ideal for LCD-related products, portable phones, CD-ROM and other miniature equipment, the FH12 offers a mounting height of 2mm and is ideally suited to high density mounting projects.
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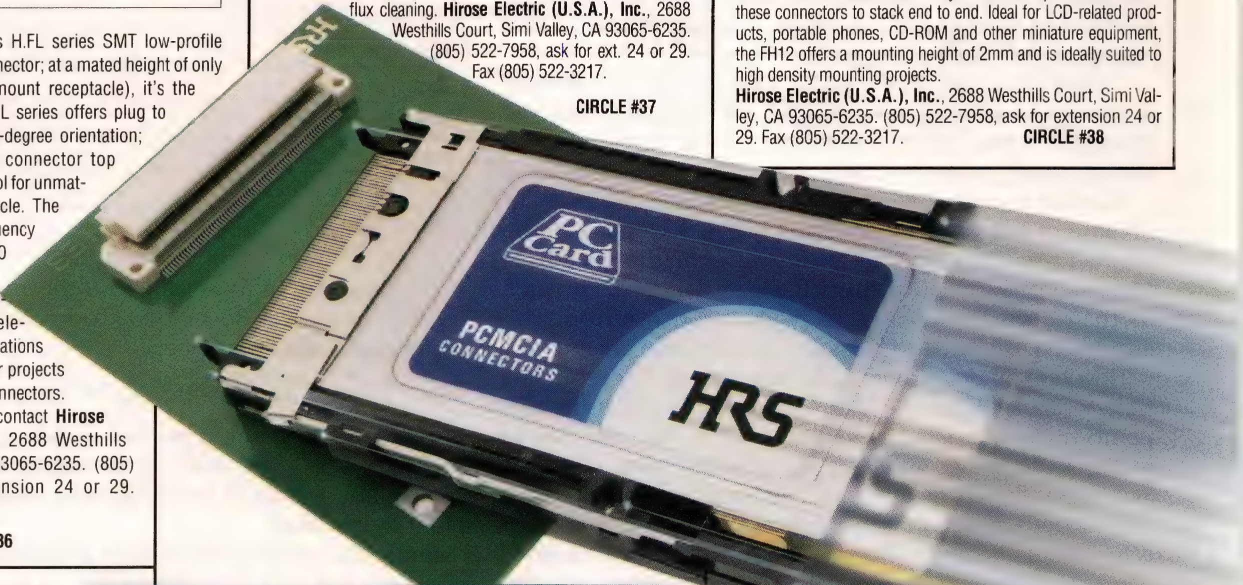
**CIRCLE #38**

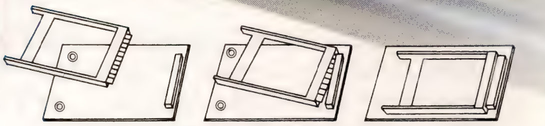


## NEW SONIC WELD PC CARD KIT

Hirose is offering the US series, an innovative sonic-weld, two-piece PC card kit which offers greater strength and lower cost of assembly. The US series is available for Type I & II, PCMCIA cards. The cost-effective kit works by simply inserting the PCB into one-half, snapping on the other half, testing the card, then sonic welding in less than a second. The US series is ideal for 88-pin DRAM cards, 68-pin memory cards and I/O cards in 9, 15, 25 and 32-positions. They are available with or without label recess.
For further information, contact the sales department, **Hirose Electric (U.S.A.), Inc.**, 2688 Westhills Court, Simi Valley, CA 93065-6235. (805) 522-7958, ask for extension 24 or 29. Fax (805) 522-3217.

**CIRCLE #39**

# PC CARD CONNECTOR UPDATE VIII



Shown is the IC8, a dual-slot, two-piece, SMT-to-board connector. The SMT portion provides full access for visual inspection of solder terminations.

Just when you thought you have seen everything in PC card connector technology, Hirose presents more surprises.

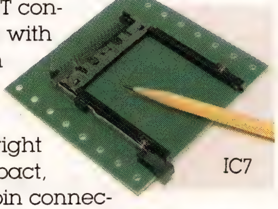
For Hirose customers, though, these compact solutions are expected. Because every day, Hirose helps design engineers package compact memory and I/O capability into sophisticated, compact electronic products.

### Dual-Slot SMT

Hirose now offers the dual-slot IC8, shown above, a two-piece SMT-to-board connector, designed for PCMCIA type I, II and III cards. The unique two-piece construction provides full access to the SMT contacts. Note in the drawings how the clip-on ejector moves in to dock with the SMT connector. Available with 2.2mm and 5mm standoffs.

### Single-Slot SMT

Shown to the right is the IC7, a compact, light-weight, 68-pin connector suitable for PCMCIA Type I, II and III cards.


IC7

About half the weight and substantially smaller and thinner than previous product, the IC7 is suitable for SMT or through-hole mounting, standard or reverse placement under the PCB and with options of left or right hand eject buttons. The choice is yours.

### Dual-Slot Through-Hole

If you are looking for alternative designs, consider the IC6 series of dual-slot PC card header connectors. These through-hole connectors are available in high-temp or value-engineered versions, and will take Type I, II and III cards.

*All of the above connectors are available in low voltage versions.* Now is the time to use Hirose PCMCIA card interconnects, with ESD and EMI protection, on your current projects.

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**CIRCLE #46**

ASIC and an FPGA is 3038 units. Therefore, if the total requirement for the above design example is fewer than 3038 units over the life of the program, the FPGA is a cheaper way to produce the devices.

One critical factor that this analysis ignores, however, is that the prototype-to-production cycle typically lasts for months. (Dataquest estimates that the average prototype-to-production time is seven months). During this time, you might use hundreds of preproduction units.

Therefore, to end your analysis here can easily lead to an erroneous conclusion. Surprisingly, the unit price and NRE charge are a small portion of the true costs. Time-to-market considerations make the most difference in total cost.

Missing a market window or delivering a product late because of long development and debug cycles can hurt a product's profitability over its life. According to a study by McKinsey and Co, late delivery has a greater impact on profits than does development or product-cost overruns. This effect is especially true in highly competitive markets.

How do you determine a late delivery cost? You can add time-to-market losses to the total product cost by using data points from your data chart (**Table 2**). The triangular model in **Fig 1**, developed by Logic Automation (now owned by Synopsys), shows the effect of delivering your product late. The model assumes that the peak of the product's earnings is in the middle of its life cycle and is independent of when you actually deliver the product. The lost revenue is the area of the large triangle less the area of the small triangle.

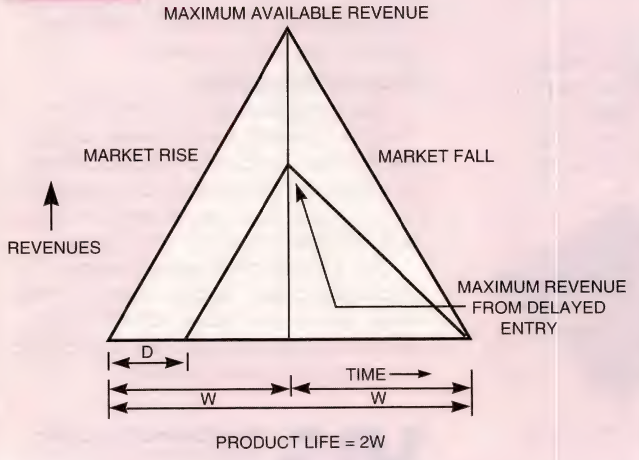
$$\text{Percentage of lost revenue} = [(D(3W-D)/2W^2)(100)]. \qquad (5)$$

From **Table 3**, the delay consists of the sum of items #17 through #27. You need 32 weeks or eight months to production to develop an ASIC. In contrast, an FPGA takes only 11 weeks or 2.75 months to production.

Because an FPGA is the faster approach to designing and delivering custom logic, the time lost building an ASIC is the difference between delivering the product with an FPGA (2.75 months) and delivering it with an ASIC (eight months), or 5.25 months, in this example. If the market for the product is three years or 36 months, the lost revenue from developing a gate array would be:

$$\text{Lost revenue} = [5.25(3*18-5.25)/36^2)*100] = 19.75\%. \qquad (6)$$

**FIGURE 1**



## TABLE 4—ASIC RE-SPIN TIME

| Stages | Weeks |
|---|---|
| Design recapture | 1 |
| Design resimulate | 1 |
| Test vector development | 2 |
| Place and route | 0.5 |
| Back annotation | 0.5 |
| Final simulation | 1 |
| Proto cycle | 2 |
| Production leadtime | 9 |
| Total time | 17 |

Therefore, even if your product generates profit at the same pace as if it had been ready at the beginning of its window, you cannot regain the time lost, and you must add that lost profit to your cost.

Selling price of end system–(cost of system*volume/year) = net profit

$$\text{Net profit} = \$2000-\$1100*(5000+12{,}000+5000) = \$19{,}800{,}000 \text{ life of program.} \qquad (7)$$

If the lost profit is as much as 19.75%, the gate array costs an additional $3,910,500. Inserting this cost into **Eq 2** changes the cost equations:

$$\text{ASIC total cost} = 25{,}000+79{,}000+3{,}910{,}500+(X \text{ units}*13). \qquad (8)$$

$$\text{FPGA total cost} = 25{,}000+(X \text{ units}*79). \qquad (9)$$

and the break-even point moves to 153,423 units.

### Additional re-spin cost

But the costs haven't finished adding up. Although average failure rate for first-time designs is only about 10%, the greater risk with most designs is that they change several times before production. These changes result from your modifying logic or fixing bugs and refabricating the device. These iterations take time and substantially raise the costs of a gate array.

Currently, roughly 30% of designs are re-spun. Using this number and assuming another $25,000 NRE charge, the probable cost of a re-spin is:

$$\text{Re-spin cost} = [(17 \text{ weeks}*\$3000 \text{ engineering per week})+\text{NRE}]*\text{re-spin potential}. \qquad (10)$$

$$\text{Re-spin cost} = [(17*3000)+25{,}000]*0.3 = \$22{,}800. \qquad (11)$$

In contrast, FPGAs require no manufacturing re-spin time, so the FPGA cost does not change. The ASIC's cost is now:

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CIRCLE NO. 122

25,000+79,000+3,910,500+22,800+(X units*13), (12)

and the break-even point moves to 154,300 units.

But this analysis fails to account for the revenue lost during the 17 weeks that you spent recapturing, simulating, prototyping, and getting the design approved (**Table 4**). The lost revenue rises to 32.6% of the total revenue, or $6,454,800, instead of the $3,910,500 before the re-spin. Break even now becomes 252,176 units.

### Inventory counts, too

Stocking inventory is necessary with custom parts because of long leadtimes, single sources, upswings in demand, and end-of-life buys. One generally accepted standard for measuring the cost of inventory is to use the current interest rate. For this example, assume the rate is 8%. Adding that into the equation, the cost becomes:

Inventory calculation = 0.08*units*price = (0.08*22,000 *13) = $22,880

Adding this into the ASIC's cost:

ASIC total cost=25,000+79,000+6,454,800+22,800 +22,880+(X units*13). (13)

In contrast to the ASIC, the FPGA does not have inventory carrying costs because it is a standard product with a short production leadtime and is available from distribution. Therefore, the FPGA equation does not change. Break even becomes 253,056 units.

Many users of ASICs require a second source because of the risk of not getting custom product from a single source. FPGAs are stocked and available from distributors, alleviating much of this danger. However, the cost of bringing on an ASIC second source is almost as high as developing the first source. The equation in this case could become:

ASIC total cost=25,000+79,000+6,454,800+22,800 +22,880+64,500+(X units*13). (14)

If the second source costs $25,000 NRE and the engineering costs are half of the original costs ($39,500), the new break-even point would be 255,537 units.

### Effects of price reductions

Most FPGA and ASIC pricing changes with time and volume. Historically, FPGA pricing has decreased 25% per year while ASIC pricing has decreased about 5% per year.

FPGA price reduction = $39*0.80 = $31. (15)
ASIC price reduction = $13*0.95 = $12.35. (16)

This price decrease moves the break-even point to 356,245 units.

An approach that provides time to market and design flexibility during the development stages of a project and offers a path to lower production costs would be better than choosing either FPGA or ASIC. Several companies offer FPGA-to-ASIC conversion to help achieve these goals. For example, by using the LCA files created during FPGA development, Xilinx can convert production-worthy FPGAs into a mask-programmed version of the FPGA design that costs as much as 60% less than the corresponding FPGA.

Replacing FPGAs with mask-programmed devices—Xilinx calls them "HardWire LCAs"—during the program's production phase has a dramatic effect on the cost of ownership. In almost all cases, the combined development speed and flexibility of the FPGA and the migration to mask-programmed parts are far less expensive than are traditional approaches. Continuing our example:

FPGA price=$39
HardWire price=$18
HardWire NRE charge=$18,000.

Assuming a conversion to mask-programmed parts beginning in Year Two, with consumption of 5000 units in the first year, 12,000 units in the second, and 5000 units in the third, the average price of the units works out to $22.77.

Average FPGA/HardWire price = [(5000 at $39+17,000 at $18)/22,000]

Move the break-even cost for the FPGA/HardWire approach against the ASIC approach to:

FPGA+HardWire total cost=25,000+18,000+(units*22.77)

ASIC total cost=25,000+79,000=6,454,800+22,800+22,880+ 64,5001+(X units*13) or 678,196 units

### Conclusions on break-even analysis

Carefully examining the total cost of an ASIC leads to some surprising observations. By far, the time-to-market cost, rather than the unit price or NRE charge, has the greatest impact on a development program. Time to market accounts for 90% of the total cost picture. Combining the FPGA with its mask-programmed equivalent for production volume moves the break-even point into high-volume areas. Other considerations, such as inventory and cost of second sourcing, add to the total cost of an ASIC program, but to a lower extent than time to market or design flexibility.

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## Author's biography

*Joseph Liu is senior applications engineer for Xilinx Asia Pacific, with responsibility for applications support throughout Asia. Liu has an EE degree from the University of Texas in Austin. He has been with Xilinx for four years, working in both the factory and the field. You can reach him at (852) 2410-2740; fax (852) 2494-7159; email joel@xilinx.com.*

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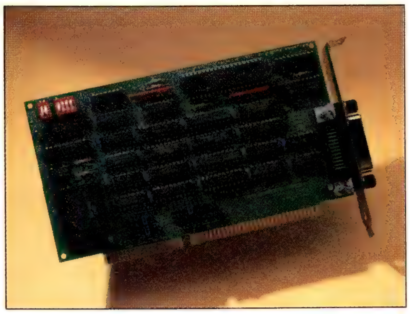

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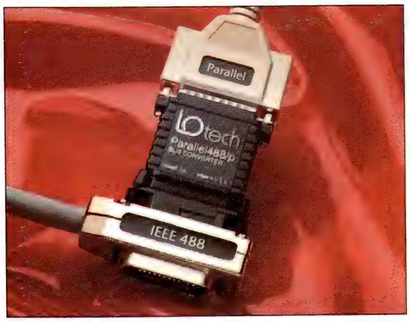

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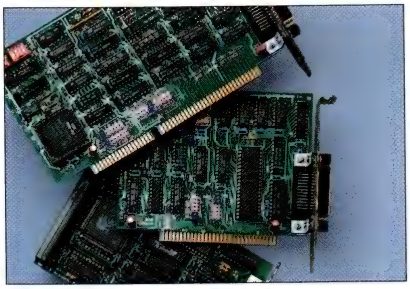

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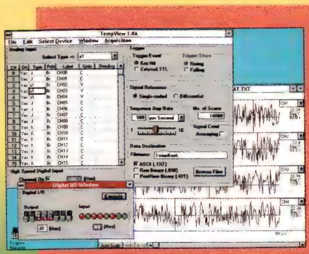

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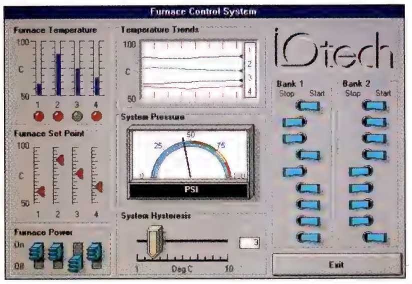

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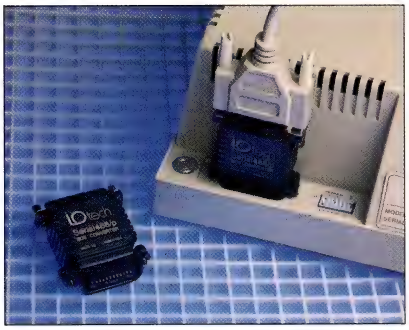

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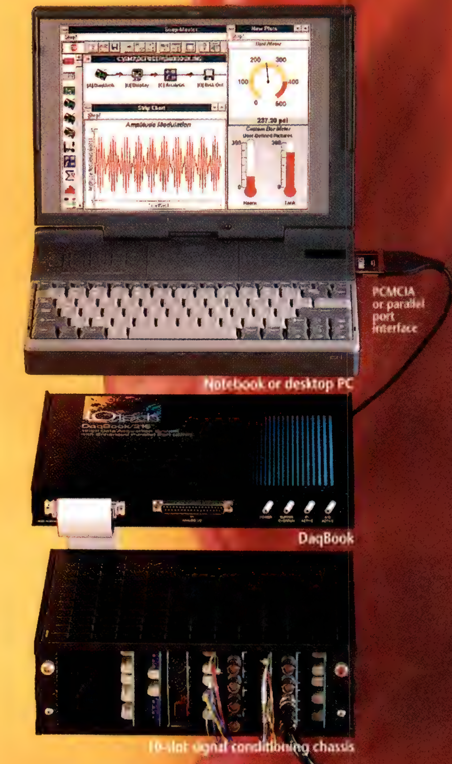
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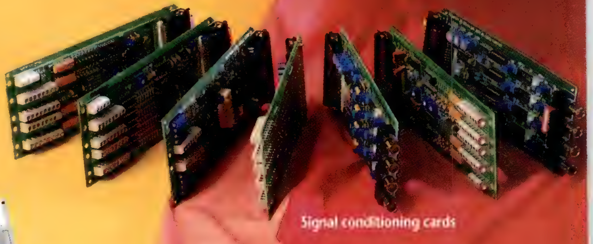

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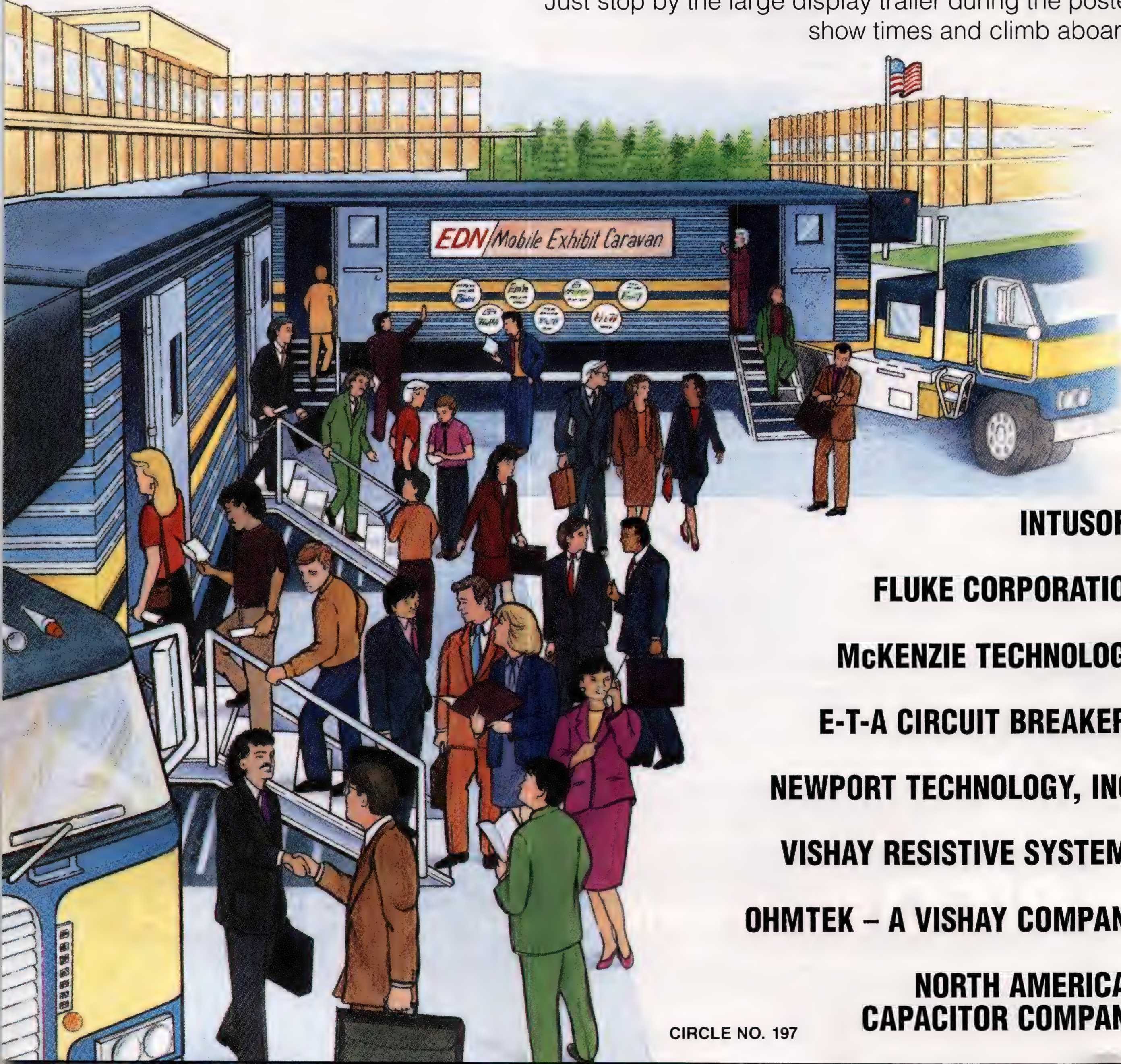

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# MOBILEEXPO'95

## Tentative Site Itinerary
## May 1 to June 16

| DATE | TIME | LOCATION |
|---|---|---|
| 5/1<br>Monday | 1:00 - 3:00<br>PM | GE PROTECTION & CONTROL<br>205 Great Valley Parkway, Malvern, PA |
| 5/2<br>Tuesday | 11:30 - 2:00<br>PM | UNISYS CORPORATION<br>2476 Swedesford Rd., Paoli, PA |
| 5/3<br>Wednesday | 9:00 - 11:00<br>AM | HONEYWELL, INC.<br>1100 Virginia Dr., Fort Washington, PA |
| 5/3<br>Wednesday | 12:00 - 2:30<br>PM | LEEDS & NORTHRUP<br>795 Horsham Road, Horsham, PA |
| 5/4<br>Thursday | 9:00 - 11:00<br>AM | KULICKE & SOFFA<br>2101 Blair Mill Road, Willow Grove, PA |
| 5/5<br>Friday | 9:00 - 11:00<br>AM | SIEMENS ROLM SYSTEMS TECHNOLOGY<br>3 Computer Drive, Cherry Hill, NJ |
| 5/5<br>Friday | 11:45 - 1:30<br>AM - PM | TELENEX COPORATION<br>13000 Midlantic Drive, Mount Laurel, NJ |
| 5/8<br>Monday | 9:00 - 11:00<br>AM | FORMATION INC.<br>121 Whittendale Drive, Moorestown, NJ |
| 5/8<br>Monday | 12:00 - 2:30<br>PM | LOCKHEED MARTIN GOV'T ELECTRONICS<br>199 Borton Landing Road, Moorestown, NJ |
| 5/9<br>Tuesday | 11:00 - 1:00<br>AM - PM | MARTIN MARIETTA CORP.<br>230 Goddard Blvd., King of Prussia, PA |
| 5/10<br>Wednesday | 11:30 - 2:00<br>AM - PM | AT&T BELL LABORATORIES<br>600 Mountain Avenue, Murray Hill, NJ |
| 5/12<br>Friday | 9:00 - 11:00<br>AM | GEC MARCONI ELECTRONIC SYSTEMS<br>164 Totowa Road, Wayne, NJ |
| 5/15<br>Monday | 9:00 - 11:30<br>AM | IBM CORPORATION<br>522 South Road, Poughkeepsie, NY |
| 5/15<br>Monday | 1:30 - 3:30<br>PM | IBM CORPORATION<br>Route 52, Hopewell Jct., NY |
| 5/16<br>Tuesday | 9:00 - 11:30<br>AM | PITNEY BOWES<br>35 Waterview Drive, Shelton, CT |
| 5/17<br>Wednesday | 9:00 - 11:00<br>AM | GENERAL DATACOMM INC.<br>Straghts Turnpike, Middlebury, CT |
| 5/17<br>Wednesday | 1:00 - 2:30<br>PM | BRISTOL BABCOCK<br>1100 Buckingham Street, Watertown, CT |
| 5/18<br>Thursday | 9:00 - 10:30<br>AM | HAMILTON STANDARD (Bldg. 1)<br>Hamilton Road South, Windsor Locks, CT |
| 5/18<br>Thursday | 11:00 - 12:30<br>AM - PM | HAMILTON STANDARD (Bldg. 3)<br>Hamilton Road South, Windsor Locks, CT |
| 5/18<br>Thursday | 1:30 - 3:30<br>PM | HAMILTON STANDARD (Bldg. 4)<br>New Britain Ave., Farmington, CT |
| 5/19<br>Friday | 11:00 - 1:30<br>AM - PM | OTIS ELEVATOR<br>5 - 15 Farmsprings Road, Farmington, CT |
| 5/22<br>Monday | 11:30 - 1:30<br>AM - PM | RAYTHEON CO., ELECTRONIC SYS. DIV.<br>1847 West Main Road, Portsmouth, RI |
| 5/23<br>Tuesday | 9:00 - 11:30<br>AM | EMC CORPORATION<br>South Street, Hopkinton, MA |
| 5/23<br>Tuesday | 1:00 - 3:00<br>PM | CHIPCOM CORPORATION<br>118 Turnpike Road, Southboro, MA |
| 5/24<br>Wednesday | 9:00 - 11:00<br>AM | G-TECH CORPORATION<br>55 Technology Way, W. Greenwich, RI |
| 5/24<br>Wednesday | 1:30 - 3:30<br>PM | THE FOXBORO COMPANY<br>33 Commercial St., Foxboro, MA |
| 5/25<br>Thursday | 9:00 - 11:30<br>AM | MOTOROLA ISG<br>20 Cabot Blvd., Mansfield, MA |
| 5/25<br>Thursday | 1:30 - 3:30<br>PM | INSTRON CORPORATION<br>100 Royall St., Canton, MA |
| 5/26<br>Friday | 9:00 - 11:30<br>AM | LTX CORPORATION<br>LTX Park @ University Ave., Westwood, MA |
| 5/30<br>Tuesday | 9:30 - 12:00<br>AM | POLAROID CORPORATION<br>565 Technology Square, Cambridge, MA |
| 5/31<br>Wednesday | 9:00 - 10:30<br>AM | AMERICAN POWER CONVERSION<br>9 Executive Park Drive, N. Billerica, MA |
| 5/31<br>Wednesday | 12:00 - 1:30<br>PM | LORAL INFRARED IMAGING<br>2 Forbes Road, Lexington, MA |
| 6/1<br>Thursday | 9:00 - 11:30<br>AM | PICTURETEL CORPORATION<br>100 Brickstone Square, Andover, MA |
| 6/1<br>Thursday | 12:30 - 2:30<br>PM | SIEMENS MEDICAL SYSTEMS, INC.<br>16 Electronics Avenue, Danvers, MA |
| 6/2<br>Friday | 9:30 - 11:30<br>AM | ANALOGIC CORPORATION<br>8 Centennial Drive, Peabody, MA |
| 6/2<br>Friday | 12:30 - 2:00<br>PM | ANALOGIC CORPORATION<br>360 Audubon Road, Wakefield, MA |
| 6/5<br>Monday | 11:00 - 1:30<br>AM - PM | CABLETRON SYSTEMS, INC.<br>35 Industrial Way, Rochester, NH |
| 6/6<br>Tuesday | 9:30 - 12:00<br>AM | AT&T NETWORK SYSTEMS<br>1600 Osgood Street, N. Andover, MA |
| 6/6<br>Tuesday | 1:30 - 4:00<br>PM | HEWLETT-PACKARD COMPANY<br>3000 Minuteman Road, Andover, MA |
| 6/7<br>Wednesday | 11:00 - 1:00<br>AM - PM | RAYTHEON CO., ELECTRONIC SYS. DIV.<br>50 Apple Hill Drive, Tewksbury, MA |
| 6/8<br>Thursday | 9:00 - 11:00<br>AM | TAU-TRON INC.<br>10 Lyberty Way, Westford, MA |
| 6/9<br>Friday | 10:00 - 12:30<br>AM - PM | SANDER COMPANY<br>95 Canal Street, Nashua, NH |
| 6/9<br>Friday | 2:00 - 3:30<br>PM | SANDERS COMPANY<br>65 River Road, Marrimack, NH |
| 6/12<br>Monday | 9:00 - 11:00<br>AM | HUGHES TRAINING, LINK DIVISION<br>Kirkwood Industrial Park, Binghampton, NY |
| 6/13<br>Tuesday | 10:30 - 1:30<br>AM - PM | LORAL FEDERAL SYSTEMS<br>Bodle Hill Road, Owego, NY |
| 6/14<br>Wednesday | 10:30 - 1:00<br>AM - PM | XEROX CORPORATION<br>1350 Jefferson Road, Rochester, NY |
| 6/14<br>Wednesday | 2:00 - 3:30<br>PM | ASEA BROWN BOVERI<br>1175 John Street, Rochester, NY |
| 6/15<br>Thursday | 10:00 - 12:00<br>AM | GENERAL RAILWAY SIGNAL<br>150 Sawgrass Drive, Rochester, NY |
| 6/15<br>Thursday | 1:00 - 3:00<br>PM | HARRIS CORP., RF COMMUNICATIONS<br>1680 University Avenue, Rochester, NY |
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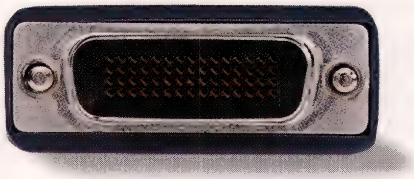

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# Simulation backplanes allow concurrent use of multiple simulators

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**Like hardware-backplane standards PCI and SCSI, the standard calls in simulation backplanes allow you to connect multiple simulators for substantial gains in design productivity.**

Modern electronic-design-automation tools provide substantial automation in design. Synthesis, automated design-layout, and complex power- and thermal-analysis tools are commonplace in today's design shops. However, verifying whether a design is correct poses mounting difficulties for designers. Advances in simulation and modeling technology and the increasing specialization of simulators have done little to reduce the design-verification effort before manufacturing. Co-simulation (**Fig 1**) has emerged as the one way to empower designers with the tools to control design verification and to achieve first-turn success with complex technologies and design requirements.

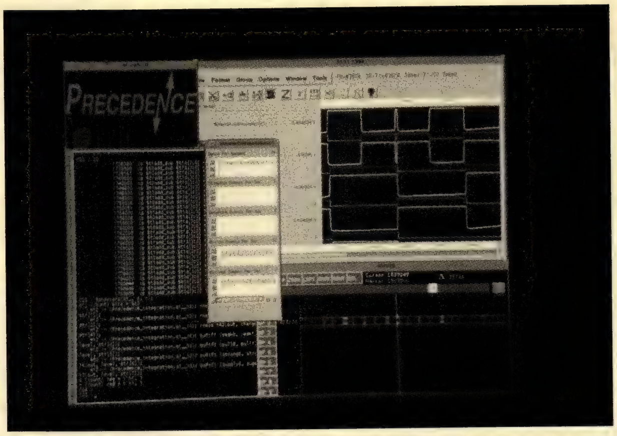
The ideal method for accurately and rapidly simulating a complex design would be to use one simulator for the entire task. With such a simulator, you could avoid the model translation, errors in interpretation, and redundant training efforts that accompany the use of multiple simulators. Unfortunately, except for simulating the simplest designs, an all-purpose simulator doesn't exist. The quest for improved performance, accuracy, and functionality has led to a dramatic specialization in simulator technologies.

Different components use different algorithms, and several hardware-description languages (HDLs) have evolved to address specialized needs. For instance, to verify the modern, complex multiprocessing computer architectures in RISC systems, a large workstation vendor has created a specialized simulator whose sole purpose is to accurately and rapidly reproduce the behavior of the workstation's CPU. The time it takes a general-purpose simulator to accomplish the same goal for even a single-CPU design would compromise the company's competitive position.

If a manufacturer proposed one all-encompassing simulator, it would need to support numerous HDLs, such as VHDL, Verilog-HDL, and HDL-Analog; several gate-level algorithms, including event-driven, leveled, and hybrid-timing; and some specialized algorithms, such as cycle, sampled-domain, and min-max-timing simulation. The designer of mixed-signal systems would also need numerous transistor-level algorithms, including Spice and switched-RC, and other complex algorithms for systems analysis, such as frequency domain. Attempts to produce such simulators have created "subset simulators" that fall short in providing coverage in any one simulation area and instead compromise either performance or—more commonly—functional completeness.

The notion of a single, do-all integrated tool is not limit-

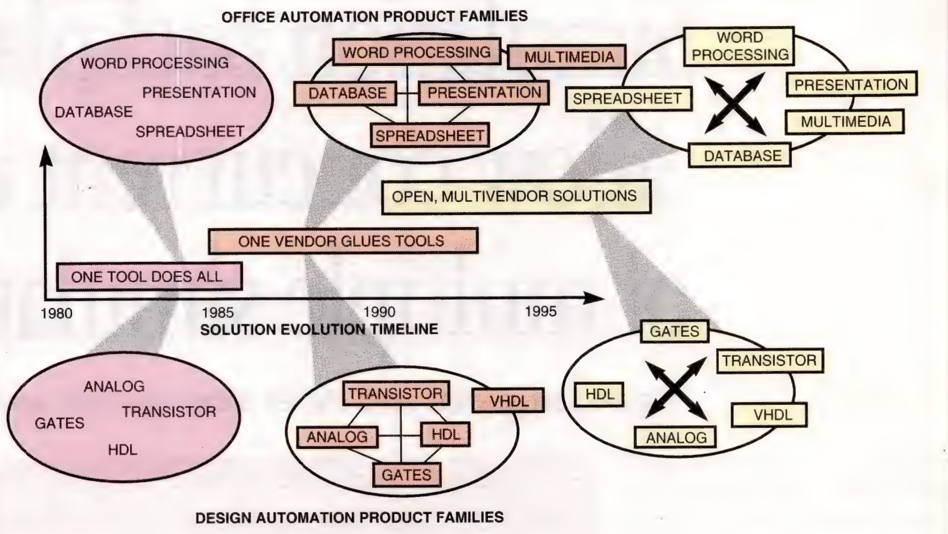
FIGURE 1



**Epic Design's Vertue co-simulation solution uses a simulation backplane to combine TimeMill transistor-level accuracy with Cadence's Verilog-XL simulator to tackle the challenges of deep-submicron design.**

ed to electronics simulation. A parallel to a single monolithic simulator ideal exists in the efforts to develop a single office-automation tool (**Fig 2**) that could operate as a spreadsheet, a word processor, a presentation tool, a calendar, and a database. The several attempts to produce such tools in the mid-1980s all failed, because the amalgamated tools were mediocre at best in each area. Such "office-automation tools" have succumbed to a family of "point tools," each excelling in its own specialty.

**FIGURE 2**



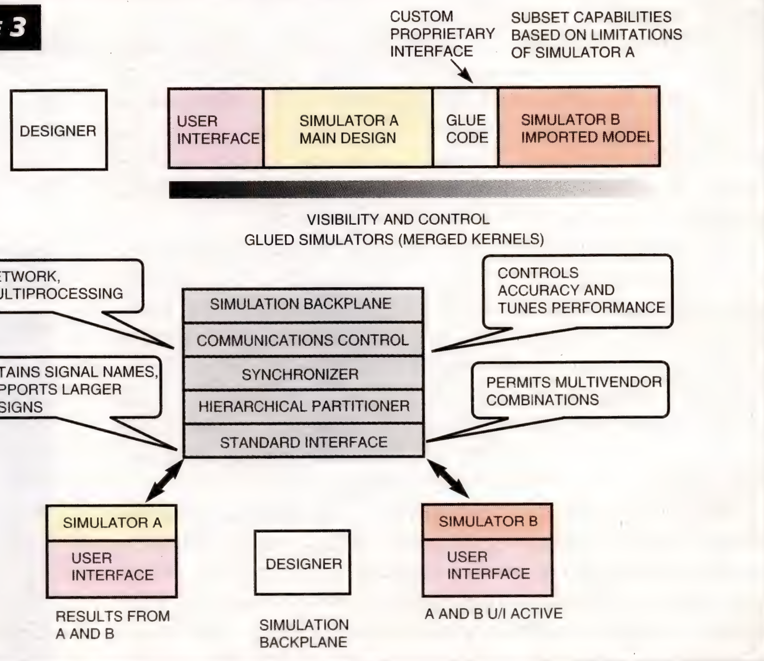
**The numerous parallels between evolutionary trends in office and design automation tools illustrate the natural migration toward open, multivendor simulation.**

## Joining simulators

The specialization of algorithms and design tasks has forced designers to use two, three, and sometimes more simulators in a design. Although the use of specialized simulators brings the benefits of each technology into the design, those benefits invoke the cost of complicating design verification. Each new simulation tool requires at least two translators—one for the design and a second for the design stimulus. If you need automatic correctness verification, common in test-bench methodologies, you must use additional translators and comparators.

To combat this nightmare of complicated conversions, designers often implement "glued" simulators, often dubbed "merged kernels," that join two simulators into a single tool or co-simulator (**Fig 3**). Design teams often employ these glued simulators as throwaway combinations. Merged kernels are custom-tailored, with substantial effort, to the design problem at hand. A design team could reuse them on a future design only if the team were redesigning the exact same part.

**FIGURE 3**



**Two popular methods of combining simulators, backplanes, and merged kernels offer designers dramatically different levels of functionality and flexibility.**

Several companies now produce commercial offerings of glued technologies. Many joinings of software simulators to hardware accelerators use glued technologies, for example. Other examples are plentiful. In the 1980s, Viewlogic introduced Viewsim/Pspice, gluing together analog and digital simulators, and Analogy introduced Saber/Cadat. And Cadence introduced the Verilog/Leapfrog glued Verilog/VHDL simulator, which replaced an earlier product, VHDL-XL.

Again, the office-automation-software analogy illustrates the evolution of multisimulators for modern, complex design problems. Once office-automation-tool developers realized

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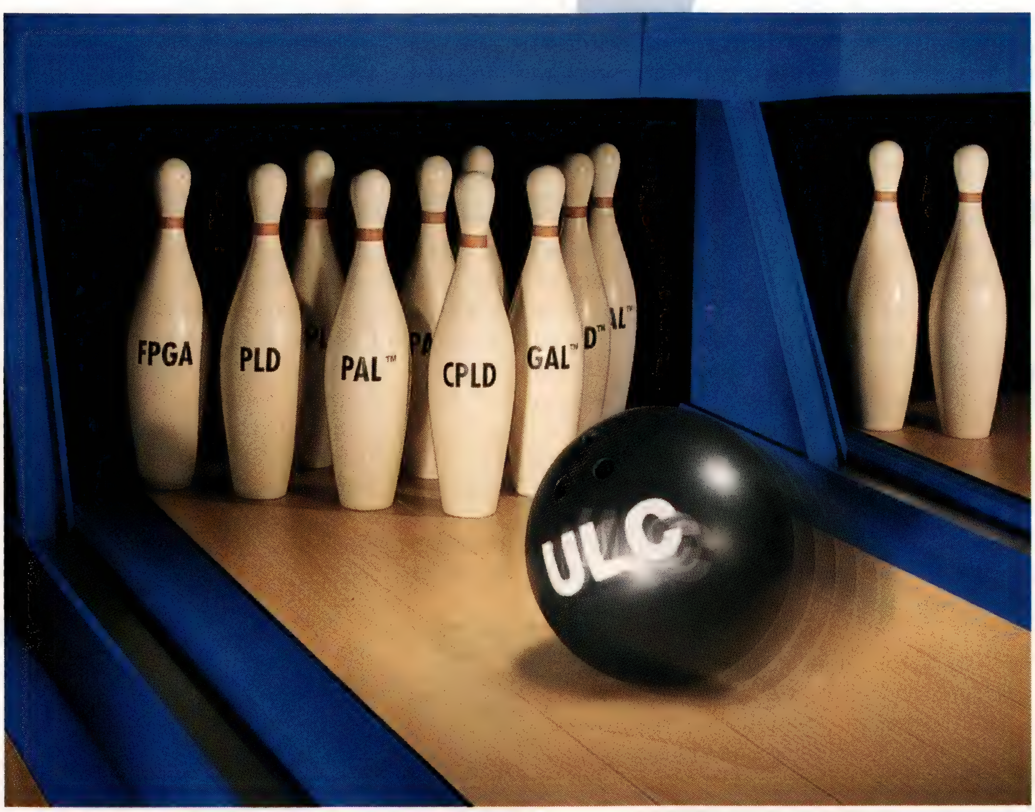

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that one satisfactory tool defied creation, each major software company developed a glued product that orchestrated multiple-point applications from that vendor into a monolithic solution.

Each vendor glued its point tools into a large conglomeration of software combining the strength of the point tool and the benefits of integration. Although the point tools from one vendor often worked together, it was impossible for a user to mix point tools from different vendors. A few vendors still market these "closed systems" in an attempt to trap users forever into the complete suite.

The development of a glued simulation requires the cooperation of the respective simulation teams from the companies involved. For example, Analogy, the provider of the Saber simulator, and HHB, the provider of Cadat, jointly developed Saber/Cadat. Even a glued solution from one company

## PERFORMANCE EVALUATION POSES TOUGH CHALLENGES

Performance continues to be of paramount concern to designers. In fact, simulation performance ranks a close second to accuracy in simulation requirements. Co-simulation is no exception to this rule. However, measuring and optimizing co-simulation performance present unique challenges to both software developers and design engineers.

Fortunately, recent advances in measuring co-simulation performance provide valuable new insights that can help designers optimally tune their co-simulators. For example, Precedence Inc's performance-analysis tool kit comprises two components. A standard-performance reference circuit (**Fig A**) that runs independently in a single simulator or in a co-simulation configuration provides raw information to the performance meter.

The performance meter (**Fig B**) measures critical co-simulation parameters and calculates and displays environment- and circuit-dependent parameters that influence performance. By combining these tools, you can determine sources of performance degradation and tune the environment, the backplane, or the circuit partition to optimize performance.

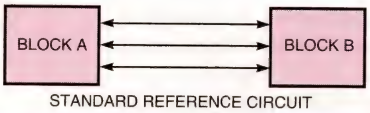
An example illustrates the use of the performance-analysis tool kit. The standard reference circuit comprises two symmetrical, equal-sized blocks. The characterization procedure requires simulating each block independently and then combining the two blocks in co-simulation. The combination effectively doubles the circuit size, stimulus, and event reporting.

The overhead expression is thus $[t_{COSIM}-t_{SIMA}]/t_{COSIM}$. The performance meter measures such critical parameters as the number of simulator synchronizations per clock and the number of mixed events per clock that a user can adjust to generate conditions at the simulator boundary.

Recently, Viewlogic Systems used the co-simulation performance-analysis tool kit to characterize the performance of the company's SimBus backplane product that links Cadence's Verilog-XL to the Vantage VHDL simulator.

"Viewlogic uniformly measured co-simulation performance approaching 90% of that of a single simulator when simulating VHDL and Verilog HDL," notes Dennis Harmon, director of technical services at Viewlogic. "These numbers were consistent whether using our own two simulators or combining simulators from multiple vendors."

**FIGURE A**

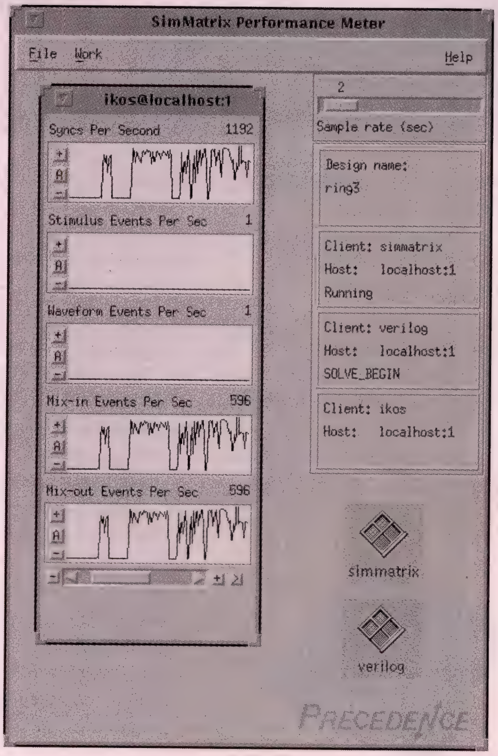


STANDARD REFERENCE CIRCUIT: 12 SYNCS/CLOCK,
32 MIXED EVENTS/CLOCK
COMMUNICATIONS: MULTIPROCESS, SINGLE CPU

| $T_{COSIM}$ | $T_{SIMA}$ | $T_{SIMB}$ | CO-SIM OVERHEAD |
|---|---|---|---|
| 93.6 | 42.7 | 42.7 | 8% |

A standard-performance reference circuit provides raw information for evaluating co-simulation performance.

**FIGURE B**



Syncs Per Second 1192
Stimulus Events Per Sec 1
Waveform Events Per Sec 1
Mix-in Events Per Sec 596
Mix-out Events Per Sec 596

Sample rate (sec) 2

Design name:
ring3

Client: simmatrix
Host: localhost:1
Running

Client: verilog
Host: localhost:1
SOLVE_BEGIN

Client: ikos
Host: localhost:1

Co-simulation performance analyzers, such as the Precedence PerfMeter, measure such useful figures of merit as simulator synchronizations per clock.

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| 03602-105-05220 | 5x7 dot matrix | 2x20 | 5mm | 5.00″ | 2.25″ | 0.88″ | 405mA |
| 03602-122-09220 | 5x7 dot matrix | 2x20 | 9mm | 7.75″ | 2.58″ | 1.00″ | 675mA |
| 03602-124-09420 | 5x7 dot matrix | 4x20 | 9mm | 7.75″ | 3.40″ | 1.00″ | 1300mA |
| 03702-020-05220 | 14-segment | 2x20 | 5mm | 5.65″ | 1.98″ | 0.82″ | 270mA |
| 03702-021-08110 | 14-segment | 1x10 | 8mm | 5.00″ | 1.60″ | 0.90″ | 140mA |
| 03702-022-13112 | 14-segment | 1x12 | 13mm | 7.20″ | 2.40″ | 0.90″ | 323mA |
| 03702-024-09116 | 14-segment | 1x16 | 9mm | 6.70″ | 2.30″ | 0.90″ | 360mA |
| 03702-026-09120 | 14-segment | 1x20 | 9mm | 8.30″ | 2.35″ | 0.95″ | 390mA |
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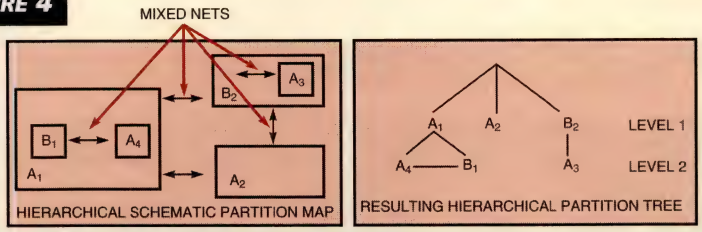
requires the cooperation of the software-development groups for each of the simulators. Because creating the glued simulation is not the primary objective of either of the teams, the simulation universally yields a product that meets only the minimum requirements for co-simulation.

The evolution of office-automation tools continues to parallel advances in multisimulation. Once office-automation users began using glued solutions from single vendors, the users craved increased flexibility, including the ability to use a combination of different vendors' point tools. The office-computing industry responded with general-purpose, open windowing systems that allow point applications from any vendor to coexist with other applications.

Multisimulator technology evolved to solve the co-simulation problem in a similar way. This technology, called a "simulation backplane," allows you to simultaneously use two or more simulators from multiple suppliers in a design session. When you use a simulation backplane, you can easily select an optimum combination of simulators for the design. You can realize substantial gains in design productivity, through either reusing design blocks or eliminating complicating translations.

Simulation backplanes allow you to interconnect multiple simulators through a set of standard calls, or "procedures." These procedures are analogous to hardware-backplane standards, such as the Peripheral Component Interconnect (PCI) or SCSI protocols. Once connected, the simulators behave as one and retain their individual qualities. The resulting simulator interoperability allows you to reuse design data, import models from an external source, and effect mixed-level simulation. Such simulation backplanes include Cadence's OpenSim, Mentor Graphics' Flexsim, Precedence Inc's SimMatrix, and Viewlogic's SimBus.

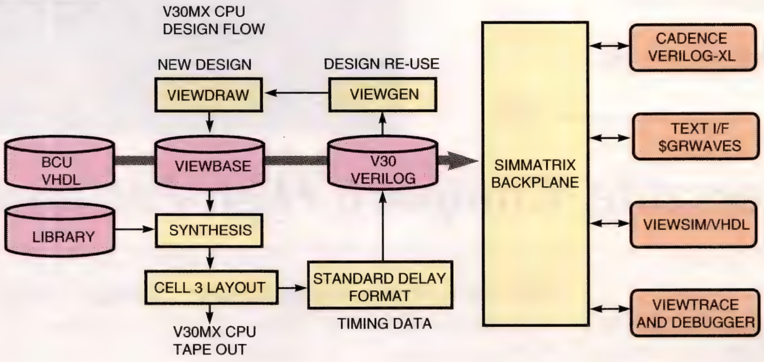
**FIGURE 4**



```
// Module instantiations ...

adder_cell unit0 (a0,b0,cin,g0,p0, sum0); // instantiation of module "adder_cell"
c1 look_ahead1 (c1, g0,p0,cin);
adder_cell unit1 (a1,b1,c1,g1,p1, sum1);
c2 look_ahead2 (c2, g1, g0, p1, p0, cin);

adder_cell unit2 (a2,b2,c2,g2,p2, sum2);
c3 look_ahead3 (c3, g2, g1, g0, p2, p1, p0, cin);

adder_cell unit3 (a3, b3, c3, g3, p3, sum3);
c4 look_ahead4 (cout, g3, g2, g1, g0, p3, p2, p1, p0, cin);

endmodule
```

**Hierarchical partitioning gives designers easy access to multiple simulators in both schematic- and language-based designs.**

**FIGURE 5**



**NEC's ASSP group used a simulation backplane to bridge the gap between Cadence and Viewlogic simulators. The result was a 20% reduction in design time.**

Simulation backplanes offer extensibility and ease of use. Unlike glued-simulator, or merged-kernel, integrations based on a simulator combination, simulation backplanes provide a simulator-independent technology. Once you make the investment in the simulation backplane, you can add simulators as the design methodologies change and the need for new circuit or process technologies arises.

Just as open windowing systems provide an easy-to-use, structured environment for combining spreadsheets, word processors, and presentation tools, simulation backplanes provide easy, natural access to the features of each integrated simulator. Unlike merged kernels that hide one simulator inside the other, backplanes provide direct access to the user interfaces of all simulators. First-time users or designers

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migrating from one design to another can choose the environment with which they feel most comfortable.

To allow simulating large or complex designs on multiple processors, a modern simulation backplane provides three communications choices: direct-link single-process, multiprocess Unix streams, and network sockets. Using these communications options, you can maximize the use of software-simulator licenses, tune the performance of the simulation environment, and take advantage of multiprocessing-CPU architectures.

Communication via multiprocessor streams or network sockets allows you to exploit "concurrence," a characteristic lacking in glued simulators and merged kernels. Concurrence allows two or more simulators to operate in parallel by exploiting the latency that results from a design partition and stimulus. Concurrence can provide significant improvements in simulation performance.

Simulation backplanes offer features that are critical in maximizing co-simulation performance and accuracy. Unlike a design that targets a single simulator, designs that contain models from multiple sources have two classes of component connections: intersimulator and intrasimulator signals. Intersimulator signals, or "mixed nets," define a boundary between components, simulators, model representations, or levels (**Fig 4**). A modern simulation backplane automatically identifies these mixed nets and creates the appropriate connections between simulators, models, or levels. As a result, a designer sees no difference between a design employing only one simulator and a design employing a simulation backplane.

Mixed nets have other significant attributes. Simulators on the backplane must synchronize timing information, in the manner of event synchronization in a logic simulator, as transitions and events are exchanged on the mixed net. The backplane software monitors each mixed net to detect transitions and to invoke synchronization algorithms. SimMatrix automatically minimizes the number of mixed nets by using hierarchical design representations and optimization algorithms. Reducing the number of mixed nets minimizes any overhead arising from monitoring mixed-net activity. In addition, the backplane offers bidirectional signal-strength arbitration and provides signal- and time-based synchronization algorithms. These features ensure accurate, real-time exchanges of information between two or more simulators.

Whether you use one simulator or multiple simulators, performance is a top priority. Optimizing multisimulator performance presents significant challenges. A backplane performance analyzer that measures critical synchronization, communication, and simulator parameters lets you maximize co-simulator performance on a variety of designs (see **box**, "Performance evaluation poses tough challenges").

Like their open windowing-system counterparts, simulation backplanes are increasingly becoming the preferred method of tackling the daunting combination of complex designs and shrinking schedules. Recently, NEC's Electronic Division reaped the benefits of backplane-based co-simulation (**Fig 5**). Given the task of designing a new high-performance μP, the NEC design team faced tight deadlines and a long list of deliverables. The team recognized that it could reuse some functional blocks from a previous version of the μP.

The NEC team switched to a new Viewlogic Powerview-based design using VHDL. The previous version of the μP used a Verilog-HDL description. Fortunately, using the SimMatrix-based ViewSim/VHDL-Verilog-XL co-simulation solution, the team enjoyed the benefits of language interoperability—between VHDL and Verilog HDL—and simulator interoperability—between ViewSim/VHDL and Cadence's Verilog-XL. As a result, the team group met its goals and realized savings of 20% in the design time of the new CPU, according to Tom Chai, senior manager of NEC's ASSP group.

Today's designers must use multiple simulators during a design. Although using a multialgorithm single simulator or gluing two simulators together may provide a short-term solution, the simulation backplane provides a strong foundation for integrating optimum multisimulators across generations of designs and simulation products.

Some of the critical features of a modern simulation backplane include hierarchical design partitioning, mixed-net identification and minimization, co-simulation performance analyzers, bidirectional strength arbitration, and distributed network co-simulation. As design complexity continues to mount and the pace of design cycles quickens, engineers will rely increasingly on the freedom to choose the optimum point simulators and combine them into application-specific solutions. EDN

## Authors' biographies

*Kevin Jorgensen is director of marketing at Precedence Inc (Santa Clara, CA). In a previous position at Viewlogic Inc, he was responsible for the introduction of the Unix-based Powerview Design Environment, as well the SimBus simulation backplane. He earned a bachelor's in electrical engineering from Duke University, Durham, SC.*

*Peter Odryna is president and chief technical officer at Precedence Inc. Previously, he held management positions in engineering and marketing at Mentor Graphics Corp and Silicon Compiler Systems. Chief architect of the SimMatrix backplane, he holds a bachelor's in electrical engineering from the University of Connecticut, Storrs, CT, and a master's in computer science from Carnegie-Mellon University, Pittsburgh.*

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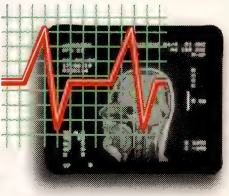

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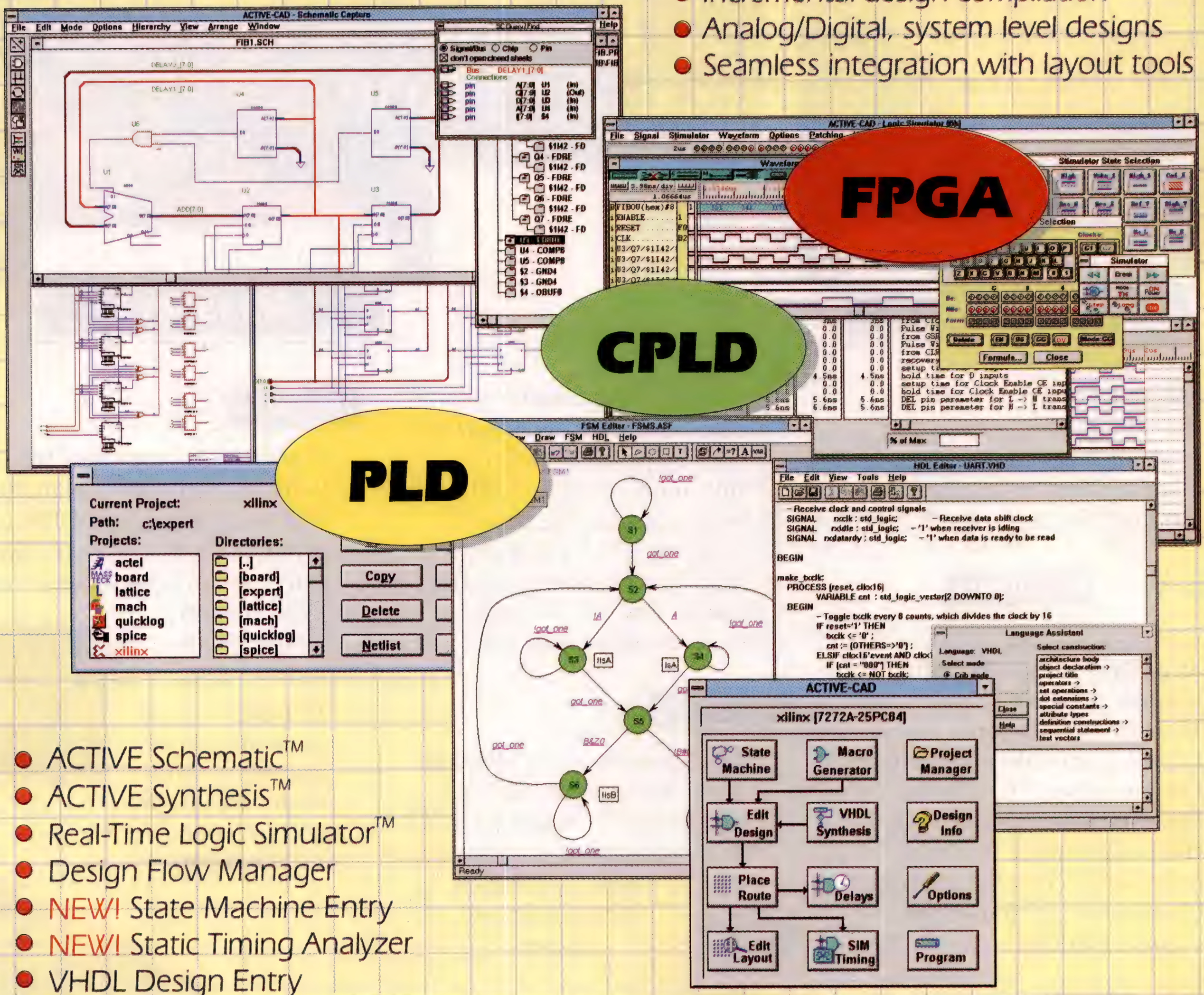

Current Project: xilinx
Path: c:\expert
Projects: actel, board, lattice, mach, quicklog, spice, xilinx
Directories: [..], [board], [expert], [lattice], [mach], [quicklog], [spice]

```
 -- Receive clock and control signals
 SIGNAL    rxclk : std_logic;          -- Receive data shift clock
 SIGNAL   rxidle : std_logic;     -- '1' when receiver is idling
 SIGNAL  rxdatardy : std_logic;    -- '1' when data is ready to be read

BEGIN

make_txclk:
 PROCESS (reset, clkx16)
        VARIABLE cnt  : std_logic_vector(2 DOWNTO 0);
 BEGIN
        -- Toggle txclk every 8 counts, which divides the clock by 16
        IF reset='1' THEN
          txclk <= '0' ;
          cnt := (OTHERS=>'0') ;
        ELSIF clkx16'event AND clkx
          IF (cnt = "000") THEN
             txclk <= NOT txclk;
```

Language Assistant
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● Crib mode
Select construction: architecture body, object declaration ->, project title, operators ->, set operations ->, dot extensions ->, special constants ->, attribute types, definition constructions ->, sequential statement ->, test vectors

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ALDEC, Inc. 3525 Old Conejo Rd. #111, Newbury Park, CA 91320. Phone: (805) 499-6867, FAX: (805) 498-7945, Email: info@aldec.com

CIRCLE NO. 10

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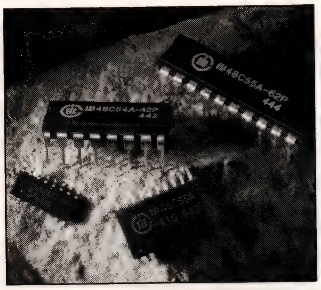
**Dual power-management switch provides the performance of discrete devices in one IC.** The MB3802 has a typical on-resistance of 0.12Ω, dropping to 0.06Ω when using parallel connections. Off-response time is less than on-response time, eliminating the need for diodes to prevent reverse current flow. The chip operates on low-input voltages, making it suitable for 3 and 3.3V systems. Available in a 16-pin SOP, the device costs $1.88 (10,000). **Fujitsu Microelectronics Inc**, San Jose, CA. (408) 922-9000.
**Circle No. 361**

**Triple-IGBT/MOS driver includes all interface functions.** The TD300 drives up to three power MOSFETs or insulated-gate bipolar transistors (IGBTs) from CMOS or low-voltage-TTL signals. The device suits motor driving, power switching, and high-voltage-level shifting applications. The chip includes three independent drivers and provides an undervoltage-lockout circuit, a current-sense comparator with alarm output, and an op amp to interface the current-sense resistor to an ADC. $0.91 (1000). **SGS-Thomson Microelectronics**, Lincoln, MA. (617) 259-0300.
**Circle No. 362**

**PCMCIA controller combines 32-bit ARM RISC processor and communications peripherals.** The VPS10101 Ruby II controller contains two UARTs, an SCC, a PIO, a two- or three-wire serial controller, high-speed SRAM, a counter/timer, and an interrupt controller. The chip provides the address, data, and control signals to implement PCMCIA and ISA interfaces. During I/O operations, the interface emulates a 16C550 communications port, providing backward compatibility with existing communications-port-based software. The chip also has four power-management modes from 30 mA at 5V for 20-MHz operation to 150 μA for fully stopped operation. The device comes in 176- and 144-pin TQFPs and costs $25 (10,000). **VLSI Technology Inc**, San Jose, CA. (408) 434-3000.
**Circle No. 363**

**Ultra-low-jitter, dual-PLL, clock-generator ICs have up to eight output clocks.** The W48C54A and W48C55A use a single external 14.318-MHz reference crystal to generate a selectable CPU clock and fixed-frequency clocks for a floppy controller, I/O chip, keyboard controller, ISA bus, and other motherboard functions. The chips generate a CPU clock and a 2X CPU clock with <1-nsec skew at frequencies up to 100 MHz. The ICs meet Intel clock specifications for Pentium and 486 processors. They also meet power-management requirements for Energy Star green PCs and operate from 3.3 or 5V supplies. The W48C54A has five clock outputs plus a rebuffered reference-clock output for video controllers and costs $2.44 (1000). The W48C55A has eight clock outputs plus two rebuffered reference-clock outputs and costs $2.67 (1000). **IC Works Inc**, San Jose, CA. (408) 922-0202.
**Circle No. 364**



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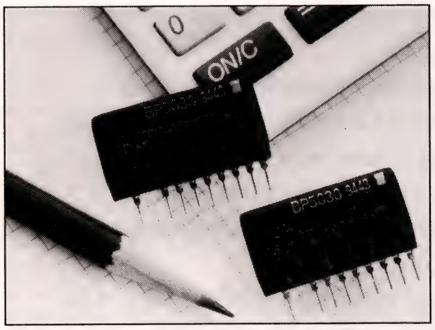
CIRCLE NO. 92

**Bus-exchanger IC interfaces between slow main memory and the fast processor pipeline.** The 54/74FCT162H272 12-bit registered bus exchanger facilitates the synchronous transmission of data to and from main memory for both RISC and CISC µPs operating at up to 100 MHz. The device has a 4.2-nsec max propagation delay and a 250-psec output skew. Balanced drive outputs and integrated series-termination resistors reduce switching noise. Minimum static current drive is ±24 mA at the guaranteed logic thresholds of 400 mV and 2.4V. The 56-pin device comes in 25- and 19.6-mil-pitch SSOPs and cerpacks. From $2.50 (10,000). **Integrated Device Technology Inc**, Santa Clara, CA. (800) 345- 7015. **Circle No. 365**



**Hybrid converts rectified line voltage to 5V dc without a transformer.** The BP5030 eliminates the need for a transformer, reducing space and weight requirements. The SIP device measures 17.9×30.5×10.4 mm and weighs approximately 2g. It requires an external diode and two electrolytic capacitors. The device works with ac sources of 80 to 120V rms at 50 to 60 Hz and provides up to 100 mA current at 5V. The low mass and the lack of a transformer provide high immunity to shock. The devices cost $2.55 (10,000). **Rohm Corp, Electronics Division**, Antioch, TN. (615) 641-2020. **Circle No. 366**

**DIMMs minimize board space and provide high density.** This 8-byte-wide dual in-line memory module (DIMM) has 168 pins and suits use with 64-bit µPs. The DIMMs are available in a 64-bit nonparity version and a 72-bit error-correction-code (ECC) version. Prices range from $245 (1000) for the 8-Mbyte THM641010AG-6/7 to $1050 (1000) for the 32-Mbyte THM72V4010-BTG-6/7 with ECC. Another version, the 72-pin SO DIMM, suits portable PCs. It mounts horizontally to the motherboard with a connector that suspends the module above the board, allowing other components to mount beneath the module. The 32-bit-wide SO DIMMs range from the 4-Mbyte THL32V1070ATG-6/7 ($150 (1000)) to the 16-Mbyte THL32V4010-BTG-6/7 ($490 (1000)). Samples are available now, and production is scheduled for the second quarter. **Toshiba America Electronic Components Inc**, Irvine, CA. (800) 879-4963. **Circle No. 367**

**350V, monolithic, MOS, power op amp available in surface-mount package.** The PA43 comes in a pinless, nonhermetic, surface-mountable DIP. It handles 350V rail-to-rail with a peak output current of 120 mA. The lightweight device measures 0.75×0.465×0.079 in. and has the die attached to the package's lid to facilitate heat dissipation. Key specifications include a 40-V/µsec slew rate and a 2-mA quiescent current. $13.60 (10,000). **Apex Microtechnology Corp**, Tucson, AZ. (602) 690-8600. **Circle No. 368**

**Photodiode and amplifier IC operates from a single supply.** The OPT101 combines a photodiode, a transimpedance amplifier, and a 1-MΩ feedback resistor in a single monolithic IC. The device suits applications such as smoke detectors, position and proximity sensors, and medical and laboratory instrumentation. It draws 120 µA from a 2.7 to 36V supply. It can also operate from dual supplies. A 7.5-mV output-pedestal voltage provides linear operation down to zero light with a single supply. Other key specifications include a bandwidth of 14 kHz and a photodiode responsivity of 0.45 A/W at 650 nm. The device is available in a clear, eight-pin DIP and a five-pin, vertical SIP. $2.55 (1000). **Burr-Brown Corp**, Tucson, AZ. (602) 746-1111. **Circle No. 369**

**10-bit, 20M-sample/sec ADC costs <$10 (OEM).** The HI5710 provides 10-bit resolution for digital video systems. The 20M-sample/sec sample rate provides four-times oversampling of 4.5-MHz video-bandwidth signals, simplifying the design of antialiasing filters used ahead of the ADC. The device features a 131-mW max operating power

**ANALOG DEVICES**
**North American Seminar**
**Locations and Dates**

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| ARIZONA | |
| Phoenix | May 18 |
| CALIFORNIA | |
| Sacramento | May 31 |
| San Diego | May 22 |
| San José | May 23 |
| COLORADO | |
| Denver | May 17 |
| FLORIDA | |
| Fort Lauderdale | June 13 |
| Orlando/Melbourne | June 14 |
| GEORGIA | |
| Atlanta | June 9 |
| ILLINOIS | |
| Chicago | May 12 |
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| Dedham | June 1 |
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| Detroit | May 16 |
| MINNESOTA | |
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| NEW YORK | |
| Rochester | June 2 |
| Westchester County | September 21 |
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| Cleveland | May 15 |
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| Harrisburg | June 7 |
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| Austin | June 15 |
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and a 5-mW power-down mode. It can drive 5 or 3.3V logic. The full-power analog-input bandwidth (–1 dB) is 70 MHz, providing a flat gain response at video frequencies. Typical signal-to-noise-and-distortion characteristics are 53 dB at 1 MHz, 54 dB at 3 MHz, 47 dB at 7 MHz, and 45 dB at 10 MHz. The device maintains 8 effective bits up to 5.5 MHz. $14.15 (1000). **Harris Semiconductor**, Melbourne, FL. (800) 442-7747, ext 7312.

**Circle No. 370**

**Low-cost clock buffers offer low propagation delay and low skew.** The CY7B9910 (TTL) and CY7B9920 (CMOS) clock buffers have a 500-psec input-to-output propagation delay and a 250-psec pin-to-pin skew. The clock drivers provide eight outputs that can drive 50Ω terminated lines. The PLL-based drivers accommodate 15- to 80-MHz clock rates and come in a 24-pin SOIC package. $4.95 (10,000). **Cypress Semiconductor**, San Jose, CA. (408) 943-2600.

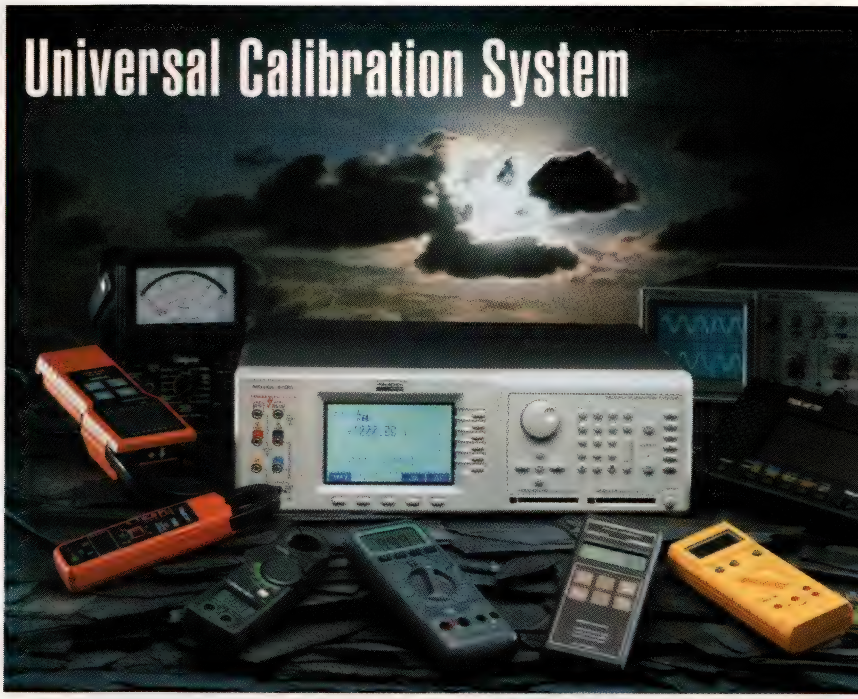
**Circle No. 371**

**Device generates encrypted signals for remote, keyless-entry applications.** The HiSec rolling-code generator provides a different signal with each transmission, offering improved security over keyless encryption systems that send a fixed code. The device randomly generates a code from $2^{48}$ possibilities, yet the coding scheme fits into only 13 bytes of memory. It costs $1.50 (OEM) for a turnkey system. **National Semiconductor Corp**, Santa Clara, CA. (800) 272-9959.

**Circle No. 372**

**In-system PLD is compatible with µPs operating at up to 75 MHz.** The 32-macrocell ispLSI 2032-150LJ has a maximum operating frequency of 154 MHz. Timing specifications include 5.5-nsec pin-to-pin logic delays, a 3-nsec input-signal setup time, and a 4.5-nsec clock-to-output time. In-circuit programming occurs through a five-wire, 5V, serial interface. The device comes in a 44-pin PLCC and costs $23.75 (1000). The traditional programmable pLSI 2031-150LJ costs $19 (1000). **Lattice Semiconductor Corp**, Hillsboro, OR. (503) 681-0118. **Circle No. 373**

**12-bit, 20M-sample/sec ADC operates on low power.** The CLC949 has programmable power consumption from 65 mW at 5M samples/sec and 220 mW at 20M samples/sec. At 20M samples/sec, the converter delivers a 65-dB S/N ratio and a 72-dBc spurious-free dynamic range (SFDR) with a 9.9-MHz analog input. Programmed for 65-mW power consumption and a 5M-sample/sec conversion rate, the device has a 67-dB S/N ratio and a 75-dBc SFDR with a 2-MHz input signal. The 44-pin PLCC is a complete A/D subsystem, including an S/H amplifier, a



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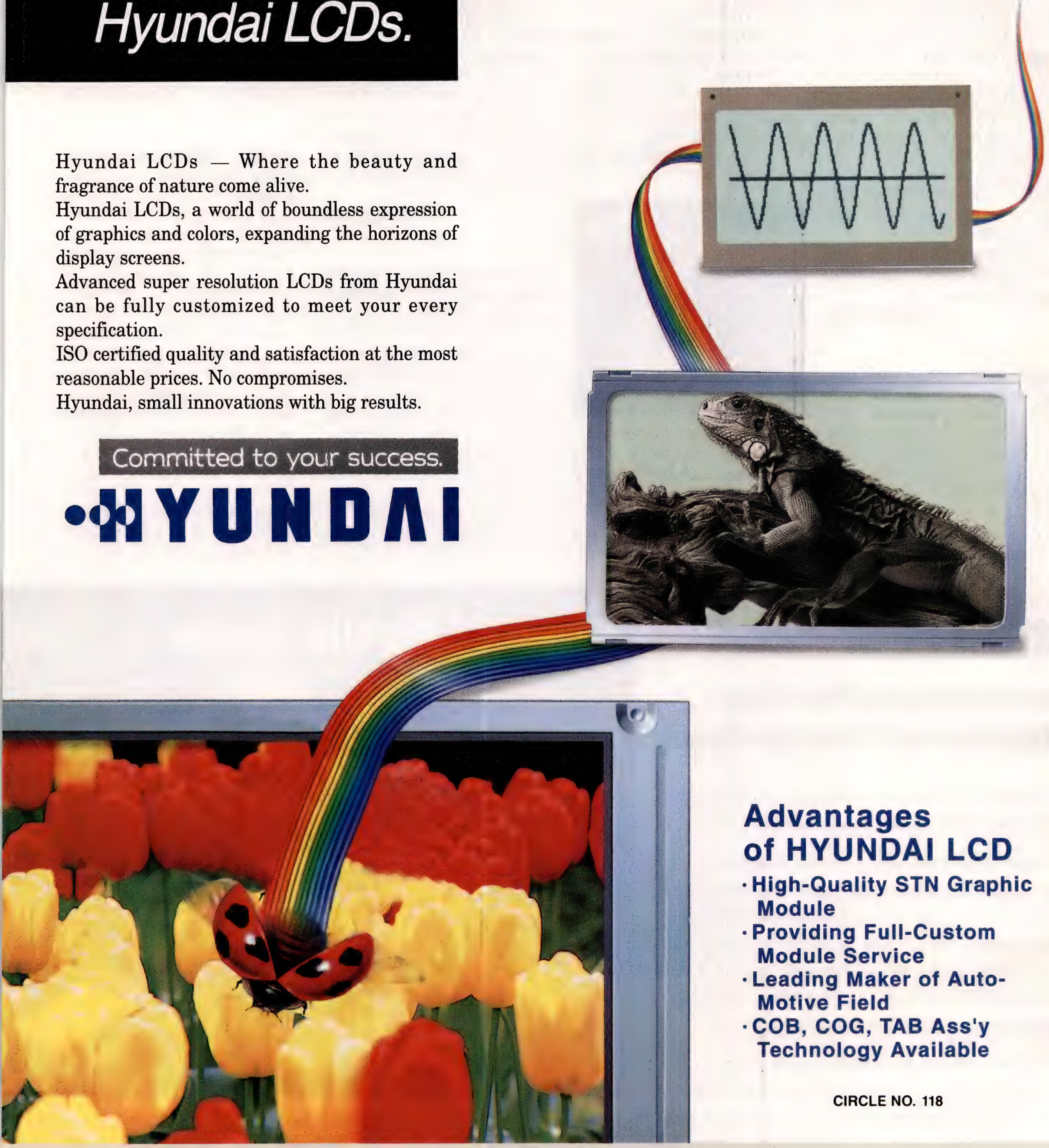

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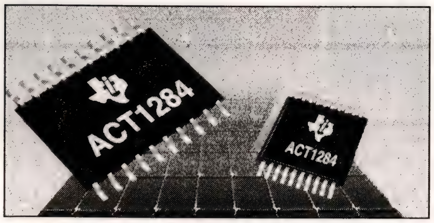
12-bit quantizer, and an internal reference. The device requires a single 5V supply and a conversion clock for operation. $98 (1000). **Comlinear Corp**, Fort Collins, CO. (303) 226-0500.
**Circle No. 374**

**8-bit, high-speed DACs for video applications.** The SPT1018, SPT1019, and SPT5140 provide word rates up to 165M, 275M, and 400M words/sec. The analog video outputs can directly drive double-terminated 50 or 75Ω loads to standard RS-343-A and RS-170 video levels. Integral and differential linearity error is rated at less than ±1 LSB. Inputs are ECL-compatible. The DACs come in 24-lead DIPs, and prices start at $20 (1000). **Signal Processing Technologies Inc**, Colorado Springs, CO. (719) 528-2300. **Circle No. 375**



**IEEE 1284 parallel-port interface has low noise.** The 7-bit SN74ACT-1284 has three-state outputs that can directly drive the IEEE 1284 communication channel. An output edge-control circuit reduces noise and signal reflections over long transmission lines. A 400-mV input hysteresis helps prevent noise and interference from being interpreted as a data signal. The device transfers data over 30 ft of cable at speeds up to 2 Mbytes/sec. The device also permits connection of a printer or peripheral to the host PC while the system is active. $0.80 (1000). **Texas Instruments Inc**, Denver, CO. (800) 477-8924, ext 4500. **Circle No. 376**

**EPLD offers 560 macrocells and in-system programmability.** The EPM9560 erasable PLD (EPLD) has up to 216 I/O pins, offers mixed 3.3 and 5V I/O, and complies with the Peripheral Component Interconnect interface. You can program each macrocell for high-speed performance or reduced power consumption. Programmable output slew rates can accelerate critical paths and reduce system noise by using slower slew rates on noncritical paths. The device is available in 208-, 240-, and 304-pin QFPs and a 280-pin PGA. The device comes in 15- and 20-nsec speeds. From $89 (OEM). **Altera Corp**, San Jose, CA. (408) 894-7000.
**Circle No. 377**

**Second-generation, 64-Mbit DRAM uses 400-mil space-saving package.** The DRAMs operate from 3.3V and are available with 50- or 60-nsec access times. The KM48V8000 is an 8M×8-bit device with 8-kbit refresh and the KM44V16000 is a 16M×4-bit device with 8-kbit refresh. Both memories are also available with 4-kbit refresh. All come in TSOP and SOJ packages and cost $600 each. Volume production is scheduled for late this year. **Samsung Semiconductor Inc**, San Jose, CA. (408) 954-7000.
**Circle No. 378**

**Two chips provide fully integrated DECT systems.** The VP23000 and the VP23001 implement the digital processing for Digital European Cordless Telecommunications (DECT) physical and media-access-control (MAC) layers. The VP23000 provides the DECT core and G.721 transcoder. In the audio interface, the core passes 32-kbps speech data to the G.721 transcoder via multiport RAM. The device also has a software-programmable radio interface and can work with industry-standard microcontrollers. The VP23001 integrates the DECT core and G.721 transcoder with an audio codec. Both parts come in 100-pin TQFP packages and cost <$10 (OEM). **VLSI Technology Inc**, San Jose, CA. (408) 434-3000.
**Circle No. 379**

**IC bridges i960 to dual PCI buses.** The CloverLeaf-960 simplifies connecting the i960 RISC processor with peripherals and add-on cards having a Peripheral Component Interconnect (PCI) bus interface. The device also allows direct communication between the two PCI buses without processor intervention. Typical applications include SCSI disk controllers, asynchronous-transfer-mode interfaces, and 100-Mbit Ethernet. The device is also useful for embedded systems using the PCI bus as a mezzanine bus and for systems requiring PCI bus expansion and traffic isolation. $68 (5000). **V3 Corp**, Toronto, ON, Canada. (416) 285-9188.
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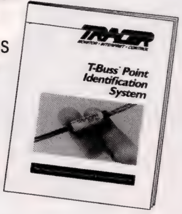

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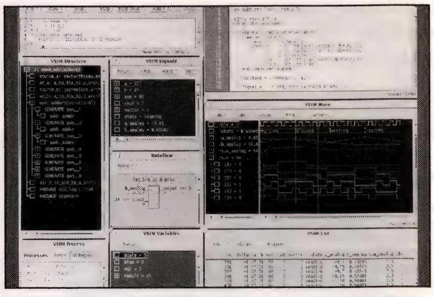
**Schematic-design tool for Windows 3.1 and Windows NT.** The WinDraft 32-bit application works with the company's WinBoard pc-board-layout tool. The software provides forward and backward annotation and post-processing functions, such as bill of materials and automatic annotation. A multiwire feature lets you draw several parallel wires simultaneously by pressing the plus or minus keys to increase or decrease the number of wires. You can also place components, such as series resistors and other passive components, on the wire; the program breaks the wire and connects the part. The tool also lets you edit any part pin name in the schematic editor without using the library editor. WinDraft costs $750, and WinDraft with WinBoard costs $1495. **Ivex Design International**, Beaverton, OR. (503) 531-3555.
**Circle No. 350**

**Windows-based pc-board-design tools come with optional autorouter.** The PCBoards for Windows pc-board-design tool manages an unrestricted number of components and pins, unlimited board size, and up to 64 board layers. The tool includes a library of >32,000 components. The 32-bit application runs under Windows 3.1 and Windows NT. Introductory price is $1079. PCBoards with Autorouter for Windows has an introductory price of $1958. According to the company, the tools are functionally equivalent to high-end PC-based circuit-board-layout packages from other vendors. **MicroSim Corp**, Irvine, CA. (714) 770-3022.
**Circle No. 351**

**New version of analog and mixed-signal simulation tool adds models and other enhancements.** PSpice Version 6.2 adds a Berkeley Version 2.0 BSIM3 model, for accurate MOSFET modeling. According to the company, the model is as accurate as proprietary models, even for short channels, over a wide range of bias levels and device dimensions. The new version also works with a variety of parameter-extraction tools, such as Berkeley Technology Associates' BSIM-Pro, HP's IC-CAP, and Technology Modeling Associates' Aurora. The simulator comes with a 32,000-component-symbol library, 10,000 simulation models, and >120 new device models. The software also has a variety of other enhancements. Prices range from $1495 to $11,900 ($1950 to $15,500 internationally). **MicroSim Corp**, Irvine, CA. (714) 770-3022.
**Circle No. 352**

**Single-kernel simulator provides seamless mixed Verilog and VHDL simulation.** V-System/Plus mixes VHDL and Verilog without two simulators and a backplane. It uses the same simulation engine with direct compile technology for both Verilog and VHDL. The software provides multiple interactive windows that let you simultaneously view and interrogate the design hierarchy, view the Verilog and VHDL source during execution, display variables and signals, control the simulator, display selected processes, and view any combination of VHDL and Verilog signals in the waveform display. The software is available for Unix workstations and costs $229,995 for a floating license. **Model Technology Inc**, Beaverton, OR. (503) 641-1340.
**Circle No. 353**



**Co-simulation with VHDL, Verilog, and Analogy's MAST languages.** Using the company's SimBus technology, you can now co-simulate with Analogy's MAST analog and mixed-signal hardware-description-language simulator, Chronologic's Verilog simulator, and Vantage's Optium VHDL simulator. Co-simulation requires a Simulation Technology interface. Prices for the interface start at $12,000 for each simulator. **Viewlogic Systems Inc**, Marlborough, MA. (508) 480-0881.
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**Verilog simulator includes interactive debugging environment.** The VCSi simulator provides analysis and

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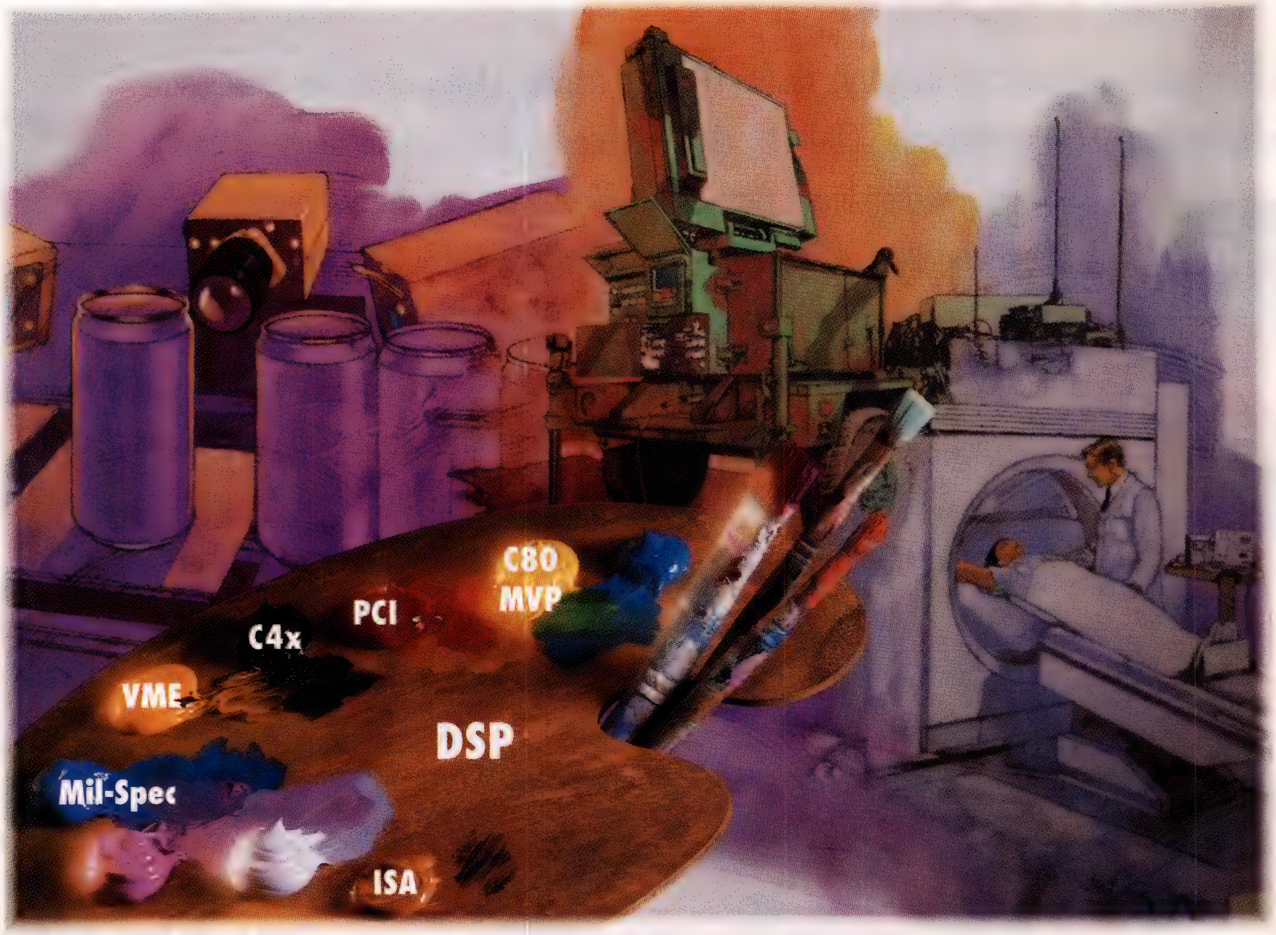

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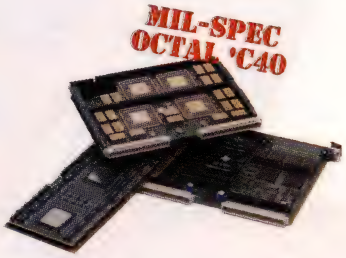

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debugging, including a design-hierarchy window to navigate the design, a waveform-display window, a source window to control and replay program execution, and a logic browser. Although not as fast as the latest version of the company's VCS product, VCSi is faster in the compilation phase, reducing debug turnaround. A floating license costs $20,000. **Chronologic Simulation**, Los Altos, CA. (415) 965-3312.
**Circle No. 355**

**Cycle-based software simulator for digital designs has 2000-cycle/sec throughput.** SpeedSim/3, according to its maker, has 10 to 100 times the performance of Verilog-XL. The simulator uses a proprietary Boolean data-flow engine to fit a 1-million-gate design into a 10-Mbyte image. The small memory requirement lets you simulate large designs on a workstation without paging. The simulator takes advantage of symmetric multiprocessing to deliver nearly linear performance gains on up to eight processors in a single system. A single networked license costs $35,000. **SpeedSim Inc**, Westford, MA. (508) 692-3737. **Circle No. 356**

**Dynamic system simulator has libraries for specialized applications.** The SystemView Simulator ($2450) has optional libraries for a variety of applications. The communications library ($875) provides communication system models, including a Reed Solomon error-correction encoder/decoder, a Costas Loop, and a PLL demodulator. The DSP library ($675) supports arithmetic modes that DSP chips use. The logic library ($525) provides models of standard-logic and mixed-signal devices, such as analog switches and DACs. The RF/analog library ($525) provides models, including, mixers, amplifier/traveling-wave tubes, RLC networks, diodes, crystal filters, delay lines, op amps, and oscillators. **Elanix Inc**, Westlake Village, CA. (818) 597-1414.
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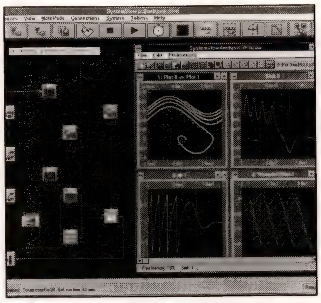

**Verification tool for multimillion-transistor, submicron IC designs.** Vampire automatically recognizes circuit structure for all design styles and hierarchy permutations and adapts itself to check the minimum set of unique instances of data. The technique fits between the time-consuming but reliable results of flat verification, which validates design data all at once, and the faster hierarchical verification, which is more difficult to set up. Because the tool requires no manual modifications to the circuit structure for verification, it eliminates introducing errors in the verification database. According to the company, the technique speeds verification by 2 to 100×. From $75,000. **Cadence Design Systems Inc**, San Jose, CA. (408) 943-1234. **Circle No. 358**

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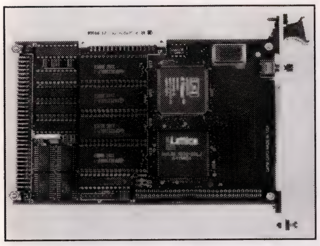
**80486 DX4-based SBC measures 5.75×8 in.** The NPC-486E single-board computer (SBC) includes interfaces for a floppy disk, an IDE port, two RS-232C or RS-485 ports, one bidirectional parallel port, a mouse, a keyboard, super VGA, Ethernet, and PC/104. A VGA and flat-panel interface provides up to 30V positive or negative LCD bias voltage, LCD-panel power sequencing, Windows accelerator implemented in hardware, up to 1 Mbyte of video memory, and a digital video-input channel. Other features include plug-and-play Ethernet configuration, up to 4 Mbytes of flash memory, and power-management features. The board costs $995 (100) with a 25-MHz 80486SX. **Adastra Systems**, Hayward, CA. (510) 732-6900. **Circle No. 335**



**ATM network-interface controller for VMEbus.** The DATM13 3U VMEbus board provides asynchronous-transfer-mode (ATM) network connection. The board uses LSI's ATMizer device as an ATM processor. The chip connects directly to the physical layer and features an internal R3200 processor executing instructions from an internal RAM to perform data structuring and movement. The board supports up to 256 virtual channels, does segmentation and reassembly, and manages contiguous and noncontiguous payloads. Because the processor boots from a socketed serial PROM, the company can update the board as all ATM adaptation-layer levels emerge. Plug-in modules support DS3, synchronous-optical-network, and E3 standards. The DATM13 costs $959 (OEM). **Dynatem**, Mission Viejo, CA. (714) 855-3235. **Circle No. 336**

**Pentium-based SBC has ISA and PCI buses.** The PCA-6156 single-board computer (SBC) comes with a 60- or 66-MHz Pentium CPU. It has a 192-Mbyte DRAM, 256-kbyte external cache, a Peripheral Component Interconnect (PCI) SCSI-2 controller, four PCI-enhanced integrated-device-electronics hard-disk-drive interfaces, two floppy-disk-drive interfaces, two RS-232C ports, one enhanced-parallel-port-compatible parallel port, an onboard keyboard connector, a real-time clock/calendar, power-on self-test diagnostic LEDs, and a 12-level watchdog timer. Prices for the board with a 60-MHz Pentium CPU start at $2350. **Advantech**, Sunnyvale, CA. (408) 245-6678. **Circle No. 337**

**Low-cost emulator and debugger for the Motorola DSP56002 and DSP-56004.** The CC-560xx command converter and QuickBug emulator/debugger cost $395 and suit audio applications. You can control the platform-independent tool through an RS-232C interface at speeds up to 38.4 kbps. The unit converts RS-232C commands from the host computer to a format compatible with the Motorola OnCE interface for on-chip emulation. The Accolade Group Ltd (Highland Park, IL. (708) 459-3024) markets the product in the United States. **Sample Rate Systems Oy**, Tampere, Finland. 358-31-3165 045. **Circle No. 338**

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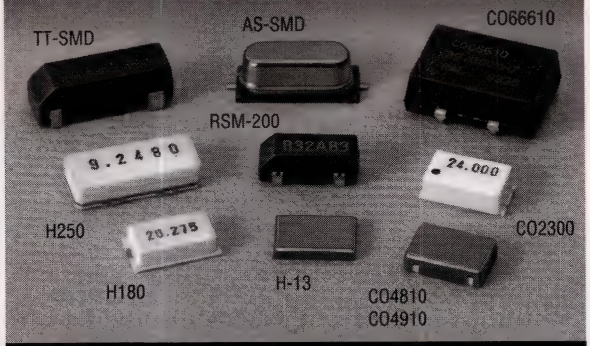

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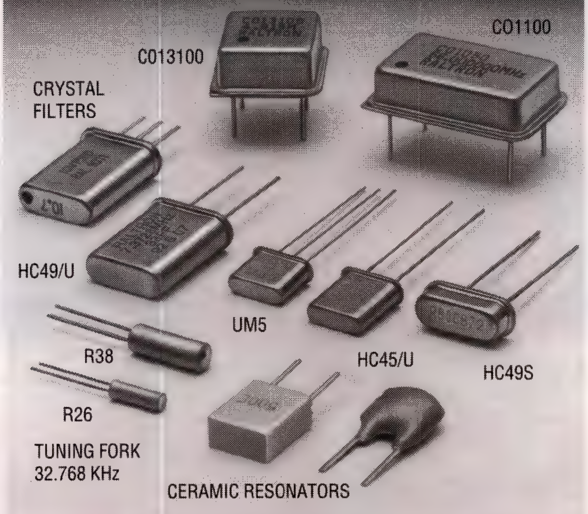

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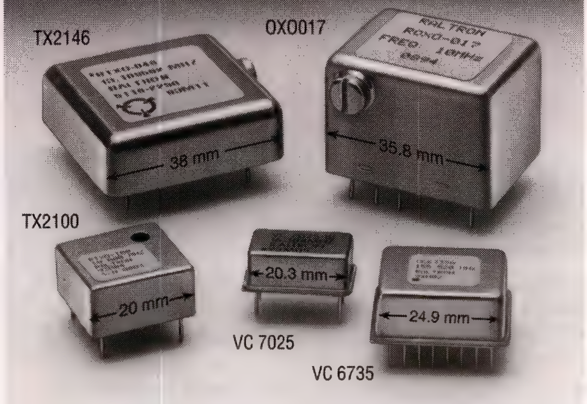

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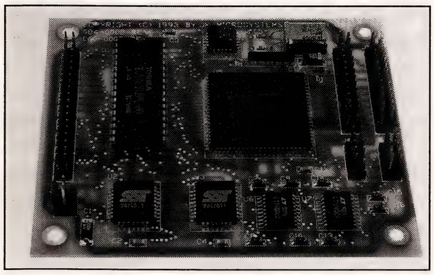
CIRCLE NO. 164

**PC/104 SBC.** The TB8680 single-board computer (SBC) is built around a Chips & Technologies F8680 processor. According to the company, the 16-bit CPU provides 386SX performance. The board has 1 Mbyte of DRAM, expandable to 4 Mbytes; 512 kbytes of EEPROM; 256 kbytes of SRAM; a 32-pin socket for BIOS, DOS, and application software; three RS-232C ports; a bidirectional parallel port; a single-channel, 10-bit ADC; keyboard and sound ports; a CGA driver for a CRT and LCDs; integral LCD and flash supply-voltage inverters; and an optional PCMCIA Type I interface. A development system that provides a 3.5-in. floppy-disk drive is also available. The board costs $958. **The Saelig Co**, Victor, NY. (716) 425-3753. **Circle No. 339**



**Low-cost SBC comes with DOS.** The Flashlite single-board computer (SBC) comes preloaded with DOS and utility software. The board implements DOS disk drives in flash memory and provides X-modem upload software on board. You can use your PC-based development tools to produce firmware for the board. The board uses a V-25 Plus processor providing two serial ports, two DMA channels, two timers, 24 parallel I/O lines, five interrupts, and eight analog comparators. The board also has 512 kbytes of RAM and 256 kbytes of flash memory. Utility software includes a flash disk-format program, a text editor, and a Tiny Basic interpreter. $149 (100). **JK Microsystems**, San Pablo, CA. (510) 236-1151. **Circle No. 340**

**PCbus-expansion board provides 80 digital I/O channels plus utility functions.** The PCIB80 uses the company's proprietary PCbus-interface scheme and has diagnostics. You can disable each buffered I/O line on power-up to float high, low, or intermediate. Open-collector output lines sink 24 mA at 5V. The board also provides a 1-MHz clock and three 16-bit timers. An optional Visual Basic driver utility provides plug-and-play installation. The board costs £195. **Arcom Control Systems Ltd**, Cambridge, UK. +44 (0) 223 411200. **Circle No. 341**

**TMS320C32 DSP evaluation board for ISA bus runs at 50 MHz.** The TIGER 32 EVM suits multimedia application development, such as modem, fax, telephony, speech, and CD-quality audio applications. It also suits C32 evaluation and algorithm development. The board has two banks of zero-wait-state memory. You can configure each bank as 32k×32, 32k×16 or 128k×8 bits. Two 16-bit analog I/O channels provide a 50-kHz sample rate. The board also has a built-in FCC-approved, standard analog-telephone interface. Software-development tools

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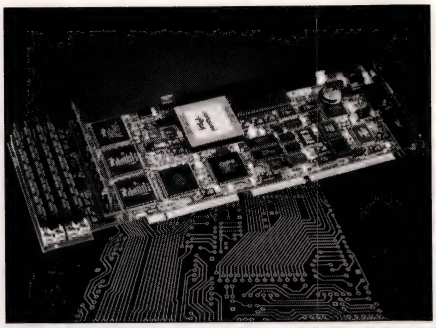
for the board include products from DSP Software Engineering, Hyperception, Momentum Data Systems, Spectron, and Tartan. The board costs $795. **DSP Research**, Sunnyvale, CA. (408) 773-1042. **Circle No. 342**

**Parallel-device programmer concurrently programs four to 16 complex devices.** The BP-2100 concurrent-programming system starts programming each device as soon it is inserted. When the last socket is filled, the first device is complete, and the process begins again, keeping the operator or autohandler busy. The system supports >7000 devices and can vector-test high-pin-count field-programmable gate arrays. Because the system is a true universal programmer, you can program virtually any device that fits into the sockets. The PLCC socket accommodates >2500 devices. The company updates the control software eight times per year. The control unit costs $4000 to $5000, and each socket costs approximately $4000 to $5000. **BP Microsystems Inc**, Houston, TX. (713) 688-4600. **Circle No. 343**



**PCI-ISA passive backplane SBC has Pentium processor.** The PCI-932 single-board computer (SBC) has a 90- or 100-MHz Intel Pentium processor. The board complies with the PCI Industrial Computer Manufacturers Group revision 2.0 industrial Peripheral Component Interconnect (PCI) specification and offers PCI and ISA passive-backplane compatibility. It has hard- and floppy-disk controllers and serial, parallel, and keyboard ports. The 32-bit PCI local bus interfaces to a Chips & Technologies F65545 video-processor chip that drives CRT screens and flat-panel displays. The board accommodates up to 128 Mbytes of DRAM, 512 kbytes of external write-back cache, and 4 Mbytes of flash EPROM. A P-90 entry-level version costs $2695. **Teknor Microsystems Inc**, Boisbriand, PQ, Canada. (514) 437-5682. **Circle No. 344**

**Log real-time task execution.** The CMXTracker works with the CMX-RTX real-time operating system to capture when a task is executing, the CMX functions called, the CMX functions' parameters, and the interrupts using CMX functions while application code is running. CMX-RTX costs $875, and the CMXTracker costs $150. **CMX Co**, Framingham, MA. (508) 872-7675. **Circle No. 345**

**Compiler and high-level-language debugger suit Zilog Z80 and Hitachi 64180.** The Z80/64180 development kit's compiler generates about

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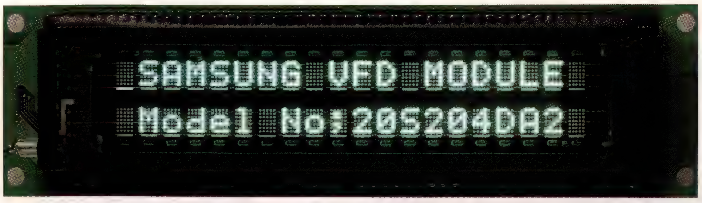

**VFD MODULES**

| MODEL | CHARACTER FORMAT & SYMBOLS | No of Digits (Row X Column) | CHARACTER DIMENSIONS | | | OUTER DIMENSIONS | | | ELECTRICAL CHARACTERISTICS | | | INTERFACE | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | CH (mm) | CW (mm) | CP (mm) | L (mm) | H (mm) | T (mm) | Vcc (Vdc) | Icc (mA) | L (Typ) (ft-L) | Parallel Input | Serial Input | Self Test | Device Select | Busy Out |
| 20S102MA4 | ▦▦▦•••••▦▦▦ | 1×20 | 5.0 | 3.5 | 4.7 | 150.0 | 30.0 | 26.6 | 5.0 | 150 | 200 | ○ | ○ | ○ | ○ | ○ |
| 20S204DA2 | ▦▦▦•••••▦▦▦<br>▦▦▦•••••▦▦▦ | 2×20 | 5.0 | 3.5 | 5.1 | 155.0 | 43.0 | 28.0 | 5.0 | 350 | 250 | ○ | ○ | ○ | ○ | ○ |
| 40S102MA4 | ▦▦▦•••••▦▦▦ | 1×40 | 5.05 | 3.55 | 4.75 | 240.0 | 40.0 | 30.0 | 5.0 | 350 | 200 | ○ | ○ | ○ | ○ | ○ |
| 40S201MA4 | ▦▦▦•••••▦▦▦<br>▦▦▦•••••▦▦▦ | 2×40 | 5.05 | 3.55 | 4.75 | 240.0 | 60.0 | 29.0 | 5.0 | 800 | 200 | ○ | ○ | ○ | ○ | ○ |
| 12L101MK1 | ▦,▦,••▦,▦, | 1×12 | 11.4 | 8.7 | 12.5 | 200.0 | 50.0 | 28.6 | 5.0 | 550 | 250 | ○ | ○ | ○ | ○ | ○ |

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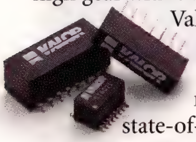

Shift your networking applications into high gear with the Fast Cats series from Valor Electronics. Each component is designed to provide a complete magnetic interface for today's state-of-the-art, high-speed LAN applications. These products reflect Valor's commitment to quality, reliability and new product development.

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The Fast Cats series provides a complete interface for the following applications: 100Base-TX, TP/PMD, 155 Mbps ATM, 100 VG-AnyLan, and 100Base-T4. These components include isolation transformer and common mode choke combinations as well as filter modules that incorporate the required filter/transformer/choke in a single package. All models provide optimized performance to support transmit and/or receive channels. Valor's Fast Cats products feature the Cougar, Cheetah and Panther series which support these high-speed applications.

| Application | Series | Part Number | Description | Package |
|---|---|---|---|---|
| 100Base-TX<br>TP/PMD<br>155 Mbps ATM | Cougar | ST6021 | Xfmr/Choke | 16-pin SOIC |
| | | PT6024 | Xfmr/Choke | 6-pin SIL |
| | | ST6025 | Xfmr/Choke/Auto Xfmr w/termination | 16-pin SOIC |
| | | PT4171 | Tx=ST6025 & Rx=ST6021 | 16-pin DIP |
| | | PT4171S | Tx=ST6025 & Rx=ST6021 | 16-pin SMD |
| | | ST6114 | Dual Choke/Xfmr/Choke | 16-pin SMD |
| | | PT4172 | Choke/Xfrm/Choke | 7-pin SIL |
| | | FL6033 | Xfmr/Filter/Choke | 7-pin SIL |
| | | SF6035 | Dual Xfrm/Filter/Choke | 16-pin SMD |
| 100VG<br>AnyLAN | Cheetah | FL6032 | Dual Filter Module | 10-pin SIL |
| | | SF6025 | Quad Filter Module | 20-pin SMD |
| 100Base-T4 | Panther | FL6031 | Dual Filter Module | 10-pin SIL |
| | | FL6038 | Dual Filter Module | 15-pin SIL |
| | | SF6036 | Quad Filter Module | 30-pin SMD |
| | | ST6111 | Quad Xfrm | 24-pin SOIC |
| | | ST6112 | Quad Choke | 16-pin SOIC |
| | | ST6115 | Quad Xfmr | 24-pin SOIC |

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25% less code than the earlier 3.21 version. The development kit comes with a new, structured assembler that includes a C preprocessor, letting you use full ANSI C macros, conditional statements, and C include files within the assembler. A relocatable linker generates PROMable code. The development kit also includes a librarian, ANSI runtime libraries, a mouse-controlled user interface, and a make utility. The full system costs $1295, and an upgrade from the previous version costs $295. **IAR Systems Software Inc**, San Francisco, CA. (415) 765-5500.

**Circle No. 346**

**Parallel-processing DSP system expands from 80 MFLOPS to multiple GFLOPS.** The system comprises the 80-MFLOPS Spirit-40 Dual VME/DSP board ($8995) and the Quad-40 VME/DSP add-on card ($8995). The Spirit-40 has two TMS320C40 DSPs, each having its own local and global SRAM. Each processor also has independent access to the card's 25-Mbyte/sec VME interface, and you can configure the processor as the VMEbus master without degrading performance. The board is based on a distributed-memory architecture, allowing it to emulate single-instruction/multiple-data, multiple-instruction/multiple-data, and data-flow architectures. The Quad-40 coprocessor board contains four TMS320C40 DSPs in a parallel structure with up to 4 Mbytes of local SRAM and shared access of up to 8 Mbytes of SRAM. Until June 30, 1995, both boards together cost $13,995. **Sonitech International**, Wellesley, MA. (617) 235-6824. **Circle No. 347**

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CIRCLE NO. 96

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**5W dc/dc converters are available in 12-pin DIP packages.** The WT series of dc/dc converters has a 2-to-1 input-voltage range, fully regulated and isolated single or dual outputs, and up to 82% efficiency. Outputs range from ±5 to ±15V in 21 models. Price is approximately $25 (OEM). **International Power Sources Inc**, Ashland, MA. (508) 881-7434.

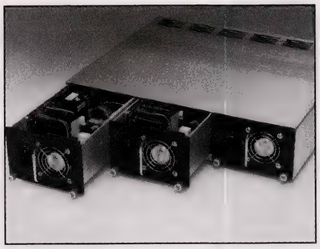
**Circle No. 383**

**Hybrid dc/dc converters offer wide-input voltage range.** The Model 3114 dc/dc converter has a nominal input-voltage range from 8 to 50V dc and is available in 11 single-, double-, and triple-output configurations. The converters are rated for 40 to 80W and come in hermetically sealed cases measuring 2.7×2.6×0.495 in. Typical performance includes dc output ripple of 50 mV p-p and efficiency ratings to 85%. The converters have an internal EMI filter that meets MIL-STD-461C. Operating temperature ranges from –55 to +85°C. A radiation-hardened configuration is also available. From $1757 (10). **Modular Devices Inc**, Shirley, NY. (516) 345-3100.

**Circle No. 384**

**60 to 120W dc/dc converters offers 84-W/in.$^3$ power density.** The AFL series of single- and dual-output dc/dc converters operates from nominal 28 or 270V inputs. For higher power output applications, internal current-sharing circuits provide even current distribution among multiple parallel converters. The converters can be synchronized to a 500- to 700-kHz clock. Features include undervoltage lockout, primary- and secondary-referenced inhibit, soft start, and load-fault protection. The converters operate over the military temperature range and offer 82 to 88% efficiency. From $720 (100). **Lambda Advanced Analog Inc**, Santa Clara, CA. (408) 988-4930.

**Circle No. 385**



**315W hot-swappable power supply operates from a 48V-dc input.** The Model 161 supply has a 36 to 72V input range and provides up to 5V dc at 40A, 12V dc at 8A, and –12V dc at 1A. Current sharing within 5% allows paralleled N+1 operation. From $295 (1000). **Conversion Equipment Corp**, Orange, CA. (714) 637-2970.

**Circle No. 386**

**Miniature dc/dc converters provide up to 3 kV at 1.5W.** The G series dc/dc converters accept a 2 to 12V input and provide an output proportional to the input. They are available in eight voltage ranges with regulation of 10% from no load to full load and ripple rated at 1%. You can further reduce output ripple by adding an external filter capacitor. The units come in a 1.5×1.5×0.63-in. package and operate from –10 to +60°C. $65. **EMCO High Voltage Supply Co**, Sutter Creek, CA. (209) 223-3626.

**Circle No. 387**

**Low-dropout regulator offers fast transient response.** The LT1584 7A linear regulator has a dropout voltage of 1.2V. The device suits use as a µP power supply in systems requiring 2.5 to 3.6V, such as the Pentium and PowerPC. Fixed-output versions are available for 3.3, 3.38, and 3.6V with a ±2% tolerance. An adjustable-output version is also available. Typical line regulation is 0.005%, and typical load regulation is 0.05%. The device comes in a TO-220 package and costs $5.82 (1000). **Linear Technology Corp**, Milpitas, CA. (408) 432-1900.

**Circle No. 388**

**Hybrid dc/dc converter has 8 to 50V input range.** The Model 3061 4 to 5W dc/dc converter delivers full rated power down to an 8V input. The converter is available in 12 configurations with single, dual, and triple outputs. It complies with MIL-STD-461C and can withstand an 80V transient surge. It comes in a 0.380-×1.08-in. case and weighs 20g. From $563 (10). **Modular Devices Inc**, Shirley, NY. (516) 345-3100.

**Circle No. 389**

**7.5W dc/dc converter has a 4-to-1 input-voltage range.** The LW7.5 series dc/dc converters are available with input ranges of 9 to 36 and 18 to 72V. Output voltages are 5, 12, and 15V. The converters are up to 86% efficient and come in a 1×2-in. package that is electrostatically shielded on six sides. Line regulation is ±0.5%, and load regulation is ±0.5%. $37 (OEM). **Polytron Devices Inc**, Paterson, NJ. (201) 345-5885.

**Circle No. 390**

**Low-cost ac/dc power supplies available in 100 to 300W power ratings.** The low-profile (1.77-in.) SV family of power supplies suits applications such as computer-based systems, peripherals, and point-of-sale and communications equipment. Features include an 85V- to 265V-ac auto-select input, class B EMI rating, and power-supply-monitoring signals. The company plans to introduce a power-factor-corrected version with the same form factor. Prices start at $166 (OEM) for a 300W model. **Lambda Electronics Inc**, Melville, NY. (516) 694-4200.

**Circle No. 391**

**DC/DC converter provides 165 to 240W with a power density of 43 W/in.$^3$.** The 24000P series, a member of the company's Power-Pak family of modules, measure 4.6×2.4×0.5 in. The modules provide current sharing, and you can parallel them for use in N+1 redundant systems. Input voltage ranges from 36 to 72 or 180 to 400V. Output voltages are 3.3, 5, 12, 15, or 24V. Input-to-output isolation is 2700V, and efficiencies are as high as 86%. The modules operate up to a base-plate temperature of 100°C and have an MTBF >1 million hours. All models meet UL 1950, CSA 22.2, and VDE 0805 requirements. The modules cost $192 (100). **Conversion Devices Inc**, Brockton, MA. (508) 559-0880.

**Circle No. 392**

**Hardware and software let you monitor and manage smart and dumb UPS systems.** NetTrax XMP runs under Novell NetWare 3.1 or higher and lets you monitor and manage uninterruptible power supplies (UPSs) on both file servers and Windows workstations. The software works with the vendor's UPSs and those from other vendors, including APC, Tripp Lite, Best, and Exide. Prices for the software start at $249.95. Prices for Agent X, a program that works with competing smart (µP-controlled) UPSs, start at $89.95. NodeTrax is similar in shape

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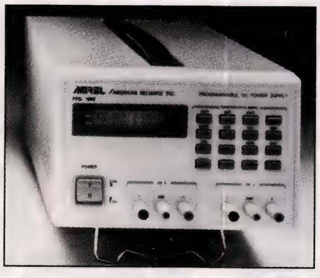
to a standard plug-strip surge protector, but it allows connection to NetTrax XMP to provide monitoring of dumb UPSs. It costs $99.95. **EFI Electronics Corp**, Salt Lake City, UT. (801) 977-9009.
**Circle No. 393**

**High-voltage power sources drive CW magnetrons from 1 to 75 kW.** You can use the 12-kW modules individually or stack them to provide high-voltage dc power from 12 to >100 kW. The supplies drive continuous-wave (CW) magnetrons for industrial heating applications. The devices allow output power to be shut down in <30 μsec after the devices receive a fault signal and then to start up again, according to a preset program. The devices use automatic ramping of the anode voltage and current to minimize magnetron stress. Efficiency is typically 90%. From $6000. **Spellman High Voltage Electronics Corp**, Plainview, NY. (516) 349-8686. **Circle No. 394**



**Low-cost programmable power supplies.** The PPS series of industrial-grade, linear, single-channel, programmable power supplies costs $895 to $1995. The devices include an IEEE-488 interface that controls power-supply functions, including calibration. The supplies also have a keypad and an LCD for local operation. You can constantly monitor voltage and current on the display. To ensure that the load receives the proper voltage and current, the supplies have a remote-sense function to compensate for lead-wire losses. The product line includes 22 models ranging from 8V dc at 10A to 250V at 0.8A. **American Reliance Inc**, Arcadia, CA. (818) 303-6688.
**Circle No. 395**

**1 to 15W encapsulated ac/dc converters offer low noise.** The PM300 and PM500 series of power converters has output ripple and noise ranging from 0.5 to 2 mV rms, depending on the model. Line regulation is ±0.02%, and load regulation is 0.01 to 0.05%. Input voltage is 115, 220, or 240V ac. The converters have an operating temperature range of −25 to +71°C and an MTBF >700,000 hours. They are available in single-, dual-, and triple-output versions with prices ranging from $70 to $130 (500). **Computer Products Inc**, South Boston, MA. (617) 268-1170.
**Circle No. 396**

**DC/DC converters provide 3.3V at 30W.** The 3003LP series of dc/dc converters has input ranges of 9 to 18, 18 to 36, and 36 to 72V. The converters feature 500V-dc input/output isolation, efficiency up to 82%,

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continuous short-circuit protection, and output overvoltage protection. Output voltage accuracy is ±1%, and line/load regulation is as low as ±0.2%. All models include a remote on/off-control input and an input π filter. The converters come in 3×2.56×0.375-in. metal cases and operate from –30 to +75°C. $95.50 (100). **Conversion Devices Inc**, Brockton, MA. (508) 559-0880. **Circle No. 397**

**5W dc/dc converters available in 24-pin DIP package.** The TP5B series dc/dc converters are available in 21 models with 2:1 input ranges from 4.5 to 72V. They are available with single and dual outputs with efficiencies from 65 to 75%. Load regulation is ±1% for single-output models and ±2.5% for dual-output models. Voltage accuracy is ±3% max. All models offer short-circuit protection and come in six-sided metal cases. The operating temperature range is –25 to +71°C. The TP5W single-output series cost $49.83 (100). **Total Power International Inc**, Lowell, MA. (508) 453-7272. **Circle No. 398**

**Dual-output, 2W dc/dc converters offer 6-kV input-to-output isolation.** The NMS series dc/dc converters operate from 5 or 12V inputs and have outputs of ±5, ±9, ±12, or ±15V. The converters offer efficiencies up to 85% and maintain full efficiency with loads as small as 1W. Output-voltage regulation is 15% or better over the full current range. The devices come in low-profile 24-pin DIP packages and operate from 0 to 70°C. $23.87 (1000). **Newport Technology Inc**, Raleigh, NC. (919) 571-9405. **Circle No. 399**

**High-reliability, 15W triple-output dc/dc converter in small package.** The MHF+28515T military-spec dc/dc converter measures 1.45×1.12×.325 in. and provides 5 and ±15V with a combined output power of 15W. The MHF+28512T provides 5 and ±12V. Both models operate over the –55 to +125°C temperature range without derating. Input voltage ranges from 16 to 48V and complies with the requirements of MIL-STD 704A. $407 (100). **Interpoint Corp**, Redmond, WA. (206) 882-3100. **Circle No. 400**

**Miniature switching-power-supply family provides outputs to 48V dc.** The company's family of miniature switching-power supplies offers 30W output and is available in a pc-board-mounting configuration ($175) or a screw-terminal configuration ($180). Regulation is better than >±0.05%, and ripple is less than 25 mV rms. The power supplies feature short-circuit protection and operate from 85 to 135V ac or 120 to 180V dc. The supply footprint is 3.5×2.5 in. **Acopian**, Easton, PA. (800) 523-9478. **Circle No. 401**

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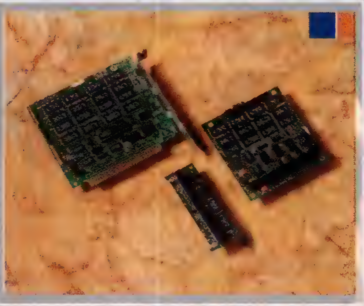

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**PC/104 IEEE 488 interface transfers data at up to 1.6 Mbytes/sec.** The PC/104-GPIB fits embedded PCs with PC/104 expansion connectors. The board is hardware- and software-compatible with the company's AT-GPIB/TNT plug-in IEEE 488.2 interface. The board comes with NI-488.2 software for DOS and Windows and is compatible with the company's data-acquisition software. $495. **National Instruments**, Austin, TX. (512) 794-0100.
**Circle No. 403**

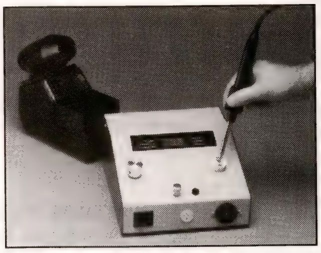
**Software tests Pentium-based PCs for floating-point defect.** The software performs 20,000 calculations to check the floating-point divide on Pentium processors. The software includes instructions for replacing flawed processors. $4.95 pays for the disk, shipping, and handling. **USA Computers/Custom Software Inc**, Lisle, IL. (708) 641-8977. **Circle No. 404**

**Benchtop tunable filter/amplifier unit has 0.1- to 49.9-kHz frequency range.** The Model 900 tunable filter provides four- or eight-pole linear-active filters in a 3.5×8.5×9.3-in. instrument. The unit is available with highpass or lowpass Butterworth or elliptic filters, and lowpass Bessel filters. Front-panel controls let you set the corner frequency, gain, offset, input selection, and bypass. The basic unit with a choice of transfer functions costs $980. Additional modules are $590 for eight-pole and $490 for four-pole transfer functions. A unit accepting battery or ac power costs $1230. **Frequency Devices Inc**, Haverhill, MA. (508) 374-0761.
**Circle No. 405**

**Data-analysis and graphical-presentation software for the PowerMac.** The Pro Fit 4.2 interactive program analyzes and represents functions and data. The tool provides interactive parameter modeling, curve fitting, spreadsheet-data management, and standard functions for scientific data analysis and graphing. $349. **Cherwell Scientific Publishing Inc**, Palo Alto, CA. (415) 852-0720.
**Circle No. 406**

**System simplifies the development and testing of PCMCIA storage devices.** The CardBench manufacturing test and development system is a self-contained test system for PCMCIA Type I, II, and III storage devices. The system includes a CPU, software, a programmable power supply, and multiple test slots for testing PCMCIA cards against PCMCIA and ATbus-attachment specifications and standards. The eight-slot CardBench 5000 system costs $17,500, and the two-slot CardBench 1000 costs $7500. **Zadian Technologies Inc**, San Jose, CA. (408) 894-0800.
**Circle No. 407**

**VLSI tester offers strobe rates to 400 MHz and drive rates to 600 MHz.** The Model 400 Vega Series VLSI tester provides a tester-per-pin architecture and is available with 32 to 384 pins. The tester offers a vector-memory depth of 4 to 64 Mbits and accommodates on-the-fly timing changes for period, edge, and format. According to the company, the MegaFlex vector-based timing subsystem lets you program a broad range of event-logic sequencing and simplifies interfacing to a variety of CAD-output formats. Typical price for the tester is $9000 per pin. **Megatest Corp**, San Jose, CA. (408) 437-9700.
**Circle No. 408**

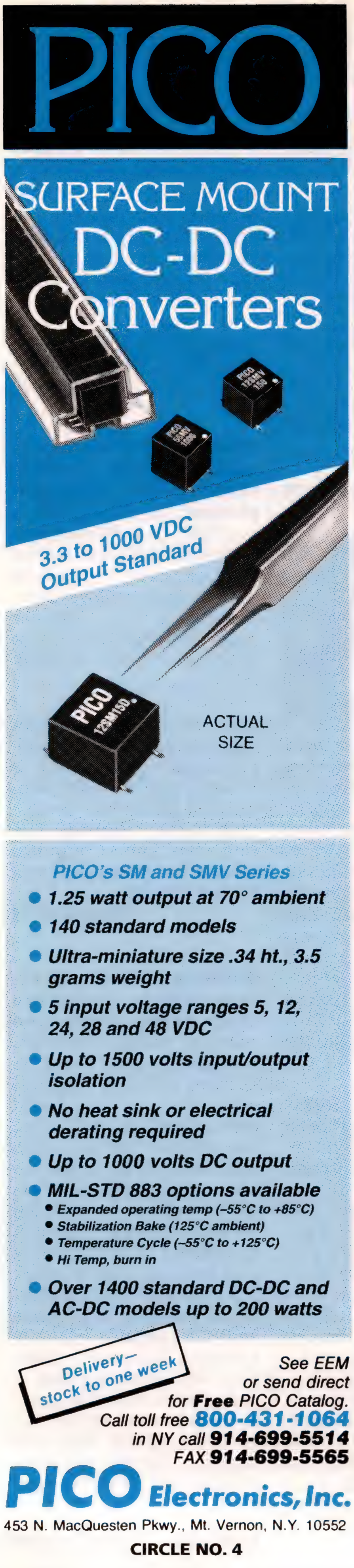


**Instrument tests and troubleshoots soldering irons.** The STS900 tests soldering irons for tip voltage, temperature, and resistance. It also tests solder pots, wave-soldering machines, and ESD-protection equipment, such as wrist straps. The standard analog output lets you record data on a chart recorder or other device. $895. **Newport Electronics Inc**, Santa Ana, CA. (714) 540-4914. **Circle No. 409**

**PCMCIA card has 16-bit ADC with sample rates to 100 kHz.** The DAQP-16, Type II PCMCIA card accepts eight differential or 16 single-ended analog inputs and is expandable to 256 inputs. The input ranges are programmable from ±0.625 to ±5V. A 512-sample data FIFO buffer enables full-speed data acquisition under various operating systems, including DOS and Windows. The card converts at full speed while using random-channel ordering and gain selection on up to 256 channels. An internal clock and divider provide accurate sampling rates from 0.01 Hz to 100 kHz. The card also provides four digital-input and four digital-output channels. The card, including software drivers and a dynamic-link library for various programming languages, costs $795. **Quatech Inc**, Akron, OH. (216) 434-3154. **Circle No. 410**

**PCMCIA card converts analog signals to 12-bit resolution at 100k samples/sec.** The PCM-DAS16 is available in a 16-channel, single-ended version and an eight-channel, differential version. Bipolar ranges are ± 0.625 to ±10V. Unipolar ranges are 0 to 0.125V to 0 to 10V. A 512-word FIFO buffer allows full-speed sample transfers of large blocks of data under Windows. Eight bidirectional digital bits supply signals for sensing or closing contacts. A programmable clock provides flexible sample-rate control. The card costs $449. **Computer Boards Inc**, Mansfield, MA. (508) 261-1123.
**Circle No. 411**

**Windows-based data-acquisition software offers configuration and control enhancements.** WorkBench PC for Windows Version 2.0 now operates with any IEEE-488 board based on the NEC 7210 chip. You can load and start alternate worksheets based on internal trigger points. You can also set the tool to latch an input based on the high or low level of another input and use setpoint triggers. The software provides historical trending, charts, date and time stamp, a sequence generator, automatic calibration, and streaming data to disk. The base edition of the software costs $995. An extended edition that adds statistics, filters, regression analysis, FFTs, and other fea-



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tures costs $1245. The runtime edition costs $329. **Strawberry Tree Inc**, Sunnyvale, CA. (408) 736-8800.
**Circle No. 412**

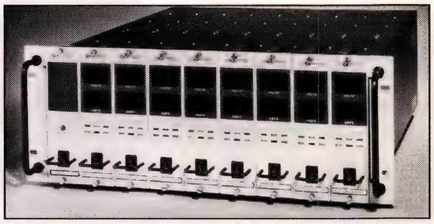
**350-MHz DSO offers four channels with high sensitivity.** The DataSYS 940 digital storage oscilloscope (DSO) has input ranges of 2 mV to 5V per division and 50k-word memory on all four channels. The instrument provides waveform analysis, including FFTs, 25 automatic measurements, and long-term archiving for later reference. Options include a 120-Mbyte hard-disk drive, a 1.44-Mbyte floppy-disk drive, a memory card, a single-ended active probe, and differential FET probes. Other options are available. Price for the four-channel DSO with color display starts at $12,295. **Gould Instrument Systems Inc**, Valley View, OH. (404) 328-7263.
**Circle No. 413**

**Oscilloscope module for logic analyzer provides two channels with 500-MHz bandwidth.** The HP 16534A oscilloscope module samples at 2G samples/sec and offers timing accuracy of ±0.005% at >150 psec. The scope module works with logic-analyzer modules in the HP 16500B mainframe to trigger a software code, state sequence, or timing to capture events. The HP 16500B logic-analysis-system mainframe costs $8980 and accommodates up to four digital scope cards. The oscilloscope module costs $11,800. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 9074.
**Circle No. 414**

**Solve calculus equations on HP 48G or 48GX calculators.** The CalcWare Series version 2 software now solves and plots equations. The software suits use by mathematics students and includes precalculus and calculus products. Each costs $39.95 and comes on a 3.5-in. floppy disk. **Sparcom Corp**, Corvallis, OR. (503) 757-8416.
**Circle No. 415**

**Two-channel, eight-pole filter provides 0.1-Hz to 200-kHz tuning range.** The Model 3382 filter is selectable between a maximally flat Butterworth filter and a linear-phase Bessel filter. Each channel can be a lowpass or highpass filter, providing an input gain from 0 to 50 dB and an output gain to 20 dB in 0.1-dB steps. The instrument has a ±10V input-signal range. Bandpass operation is available by connecting the filters in series, and band-reject operation is available by connecting the filters in parallel. The instrument costs $1695. An option extends the frequency range down to 0.005 Hz. **Krohn-Hite Corp**, Avon, MA. (508) 580-1660.
**Circle No. 416**

**ISA bus card provides 16 optically isolated inputs.** The ISOI-16 provides 2500V isolation. You can select interrupts on a per-line basis and program the lines to be enabled for high- or low-signal levels. The board uses 4 bytes of I/O space. It costs $149. **Berkshire Products**, Duluth, GA. (404) 271-0088.
**Circle No. 417**

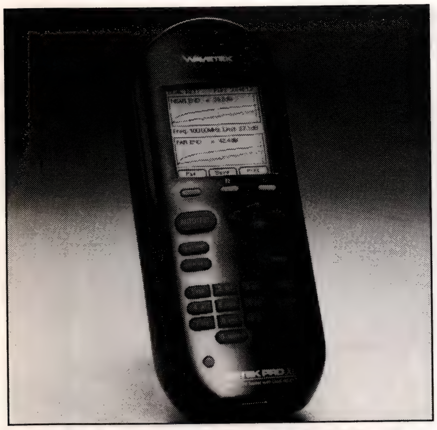


**200W programmable power supply is less than 2 in. wide.** Nine of these slim, programmable power supplies fit into a standard 7×19-in. rack housing. Each module is independent of the housing and can operate alone. You can insert and remove the modules from the front for N+1 redundancy. Eight supplies are available ranging from 0 to 6V at 20A to 0 to 150V at 1.2A. Each module has a serial interface for communication with other instruments, including VXI. The modules accept an 85V- to 264V-ac input and meet IEC 555.2 requirements. Each module provides polarity selection and output on/off relays. The modules cost $1695 each. **Kepco Inc**, Flushing, NY. (718) 461-7000.
**Circle No. 418**

**Graphics tool kit builds real-time displays under Windows in C and C++ or Visual Basic.** The Real-Time Graphics Tools for Windows let you create real-time process control, scientific instrumentation, and monitoring displays for Windows, Windows NT, and Windows 95. The base version includes 16- and 32-bit dynamic-link libraries. The tool kit contains a collection of dynamic graph types, which you can update in real time with smooth scrolling. The software provides >300 functions. There are no royalties or run-time fees. The base version costs $600 for C/C++ and $500 for Visual Basic. The advanced developer's version costs $1200 for C/C++ and $1100 for Visual Basic. **Quinn-Curtis Inc**, Needham, MA. (617) 449-6155. **Circle No. 419**

**Digital termination panels offer quick-disconnect feature.** 3U-size digital termination panels with the quick-disconnect feature are available for digital relay output panels ($205), digital isolated input panels ($235), and optically isolated panels ($130). **Intelligent Instrumentation Inc**, Tucson, AZ. (602) 573-0887. **Circle No. 420**

**Frequency-analysis software lets you specify a range of FFT window widths.** Snap-Master frequency analysis version 3.0 lets you specify window widths whose prime factorial includes an even combination of two, three, five, and seven up to 16,384 data points. The tool provides >300 FFT window widths instead of the eight typical for products restricted to powers of two. The software also provides 23 window types. A stand-alone analysis package costs $495 or comes with Snap-Master's data-acquisition module for $995. **Hem Data Corp**, Southfield, MI. (810) 559-5607. **Circle No. 421**



**LAN cable tester for 100-MHz Category 5 networks.** The Lantek Pro XL cable tester suits the installation and troubleshooting of Category 5 cabling for asynchronous-transfer-mode and other high-speed applications. The handheld instrument has a 40-sec test speed. Tests include crosstalk at both ends of the cable, line mapping, signal attenuation, dc-loop resistance, mutual capacitance, and cable length. The instrument also calculates the attenuation-to-crosstalk ratio. It automatically tests categories 3, 4, and 5 cable on one-, two-, three-, and four-pair unshielded-, foil-, and shielded-twisted-pair cable and on coaxial cable. $4495. **Wavetek Corp**, San Diego, CA. (619) 279-2200. **Circle No. 422**

**Handheld transmission-line DMM tests two- and four-wire telecommunication transmission lines.** The Telesense 1000 measures line loss, frequency response, and background noise. The instrument also provides a 20-kHz frequency counter and 404-, 1004-, and 2840-Hz signal-generator tones. Other features include true rms measurements and basic DMM features, such as ac/dc voltage, dc, and

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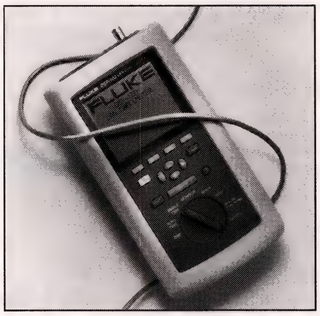
resistance. The unit has a 3½-digit LCD and can withstand 10-ft drops. $495. **American Reliance Inc**, Arcadia, CA. (818) 303-6688. **Circle No. 423**

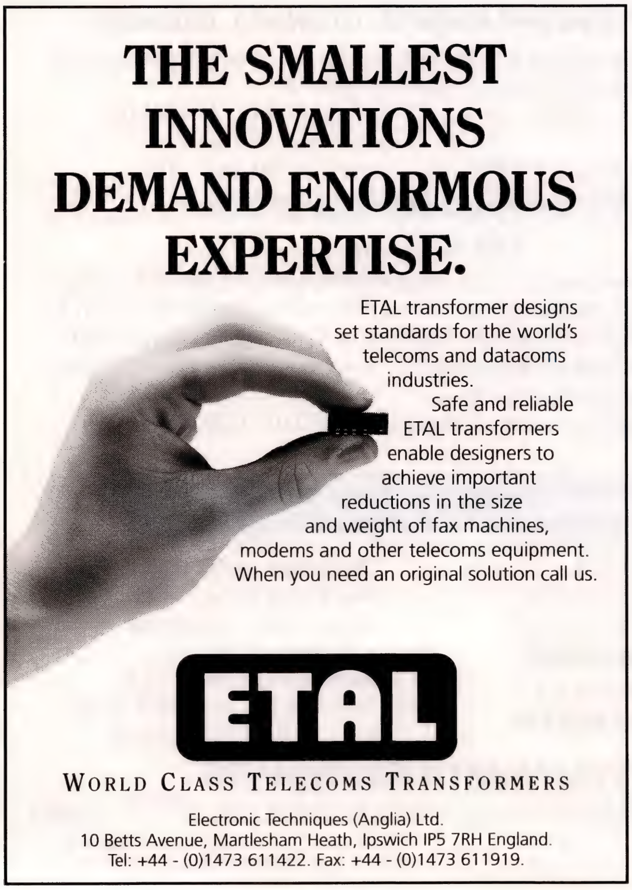
**Universal device programmer supports a variety of products.** The All-Max+ programs PLDs, including the Advanced Micro Devices Mach family; bipolar PROMs; EPROMs and EEPROMs to 16 Mbits; microcontrollers, such as the Microchip PIC series, the Motorola MC68XXX, the Zilog Z86 series; serial EPROMs; and serial EEPROMs. The programmer interfaces with a PC through a parallel port or a high-speed parallel interface card. It has a 48-pin ZIF socket for programming DIPs; a gang-programming option; and optional socket adapters for PLCC, SOIC, and SMD devices. The programmer comes with a lifetime of free software upgrades via the vendor's bulletin-board system. The programmer costs $745, including software, cable, and manuals. **Electronic Engineering Tools**, Sunnyvale, CA. (408) 734-8184. **Circle No. 424**

**IEEE-1149.1 JTAG boundary-scan controller board for ISA bus supports four independent JTAG ports.** The PC-1149.1/100F lets you apply scan vectors to as many as four scan chains. The controller accommodates scan-chain lengths up to 4 Gbits and a TCK speed of up to 25 MHz. The board also includes RS-422 support for hierarchical multidrop scan architectures, such as National Semiconductor's Scan bridge. The board also includes 16 bidirectional digital I/O lines for non-scannable nodes on the unit under test. $2950. **Corelis Inc**, Cerritos, CA. (310) 926-6727. **Circle No. 425**



**Digital cable tester for Category 5 cable testing.** The DSP-100 LAN CableMeter is a handheld tool for testing installed Category 5, ISO and IEC LAN cabling to 100 MHz. The tester uses DSP technology to provide high accuracy, high test speed, and fault identification with location of crosstalk faults. The unit performs a cable test in 20 sec. It costs $3795. With a smart remote unit for measuring near-end crosstalk at both ends of the cable, the tester costs $4995. **Fluke Corp**, Everett, WA. (206) 347-6100 **Circle No. 426**

**LCR meter has 1-GHz frequency range.** The HP 4286A measures inductance, resistance, and capacitance (LCR) from 1 MHz to 1 GHz with 10-kHz resolution. The meter's impedance ranges from 200 mΩ to 3 kΩ, and basic accuracy for impedance is 1%. Test signals range from 10 mV to 1V. The instrument requires 15 msec per measurement. $27,600. **Hewlett-Packard Co**, Santa Clara, CA. (800) 452-4844, ext 9150. **Circle No. 427**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**Command translator lets you use IEEE-448 to control proprietary bus.** The GAT-1 translates IEEE-488 commands to the Audio Precision Interface Bus (APIB) commands. The unit lets owners of APIB-based System One units operate them through an IEEE-488 controller. The command translator costs $1850. **Audio Precision**, Beaverton, OR. (503) 627-0832.
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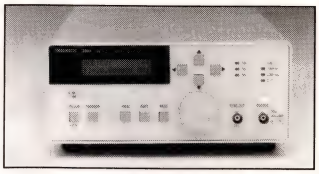
**Data-acquisition boards for PC/104 offer 12- and 16-bit resolution at 100k samples/sec.** The 12-bit AIM-12-1/104 ($365) and the 16-bit AIM-16-1/104 ($625) have 16 single-ended or eight differential analog input channels and 16 digital I/O lines. The 16-bit board provides 85 dB of spurious-free dynamic range (SFDR) with input ranges of 10, 5, 2.5, and 1.25V. The 12-bit board provides 75 dB of SFDR with input ranges of 10 and 1V and 100 mV. They are available with bipolar or unipolar ranges. **Analogic Corp**, Peabody, MA. (508) 977-3000. **Circle No. 429**

**Direct-digital-synthesis function generator for communications product testing.** The Model 1404A function generator lets you select frequency, amplitude, and modulation directly from a knob- and key-controlled front panel. Cursor controls let you identify the active parameter on the display for editing. The instrument has a 10-mHz frequency resolution and a 100-mHz to 20-MHz frequency range. Both sine- and TTL square-wave outputs are simultaneously available. A variety of modulation types is available, including binary phase-shift keying, quadrature phase-shift keying, 8 phase-shift keying, and quadrature amplitude modulation (QAM). The instrument digitally implements QAM. You can phase-lock two or more instruments and control the phase angle independently. The instrument costs $1295, including RS-232C and IEEE-488.2 interfaces. **Pragmatic Instruments Inc**, San Diego, CA. (619) 271-6770.
**Circle No. 430**



**Floating-point DSP board for PCs costs $595.** The DSP platform uses the 32-bit TMS320C32 DSP. It is source- and object-code-compatible with other members of the TMS320C3X family and source-code-compatible with the TMS320C4X family. The board includes a stereo 16-bit A/D D/A converter and 128 kbytes of zero-wait-state SRAM. A bytewide DRAM interface lets you add up to 16 Mbytes of low-cost SIMM. A software-developer's kit is available with the TI TMS320 floating-point DSP optimizing C compiler, TMS320 floating-point DSP assembly-language tools, a C source debugger, a real-time I/O system providing memory management, real-time device-independent I/O drivers, and a host/DSP communication system. **Atlanta Signal Processing Inc**, Atlanta, GA. (404) 892-7265.
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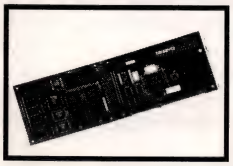

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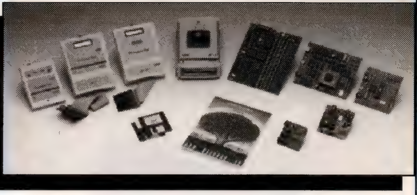

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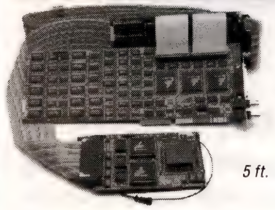

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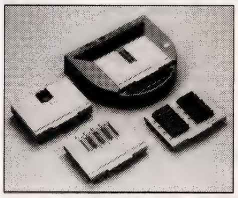

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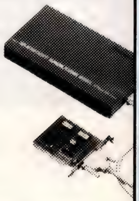

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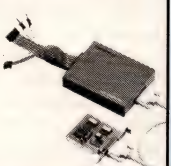

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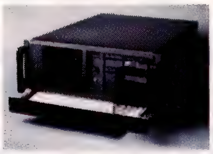

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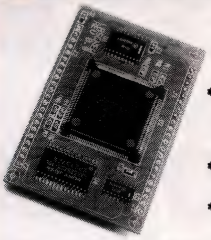

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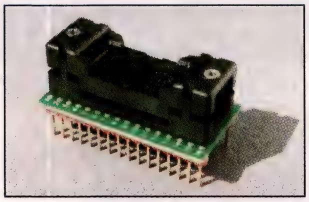

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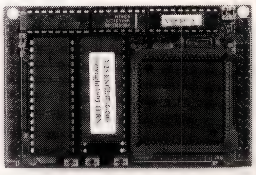

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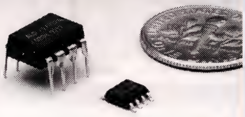

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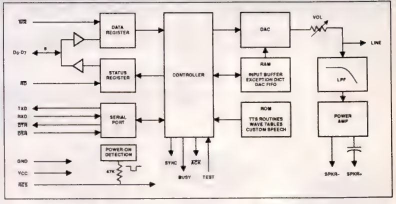

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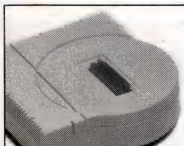

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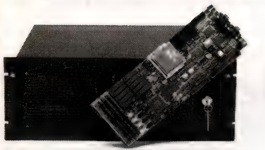

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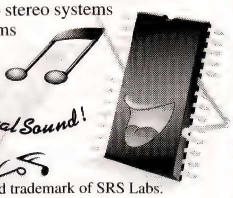

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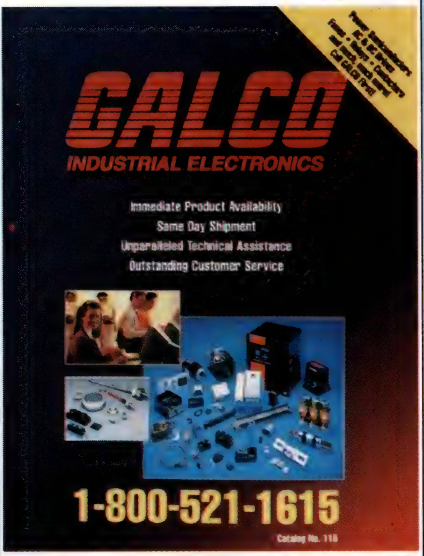

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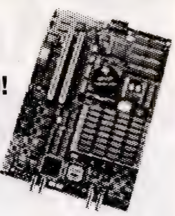

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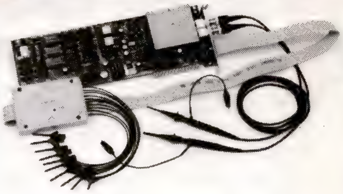

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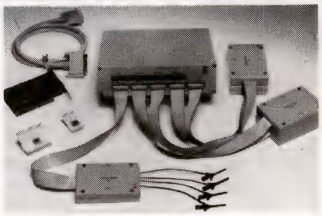

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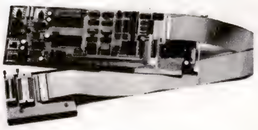

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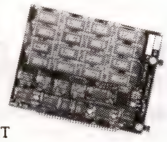

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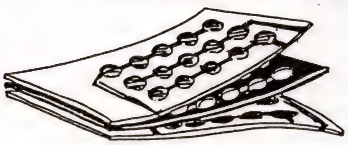

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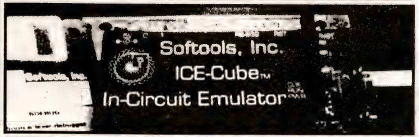

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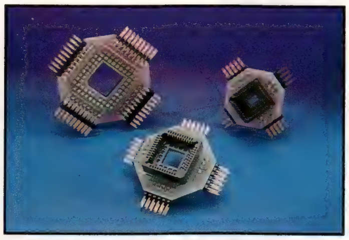

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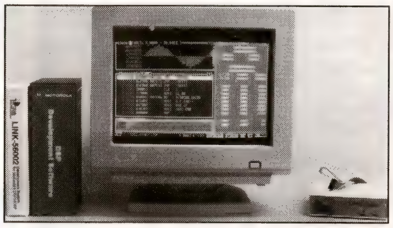

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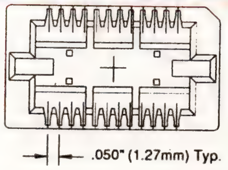

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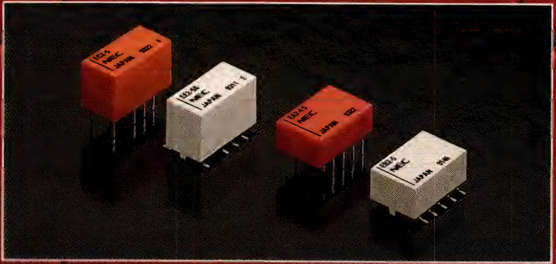

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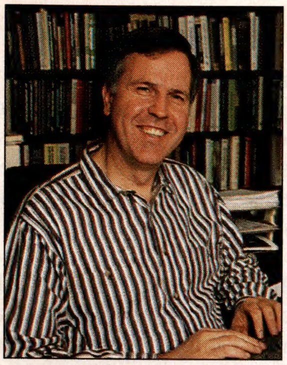

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# Fuzzy logic: an enabling technology

Many of the attacks leveled against fuzzy logic seem to support the time-honored axiom that ignorance is the firmest basis from which to criticize. Some, however, are well-considered. One observation in particular—I have read it in various places—is worth looking into. Simply stated, it is: *Successful applications of fuzzy logic are successful because of factors other than the use of fuzzy logic.*

Although the following response is subjective, I hope my observations are honest. I base them on the approximately 20 fuzzy design projects with which I have been directly involved, ranging from simple control systems to rather complex analysis models. In each case, the goal was not to solve the problem using fuzzy logic, but rather to solve the problem successfully and in a cost-effective manner. In each case, the solution included fuzzy logic.

## What does fuzzy provide?

Two widely claimed benefits of fuzzy systems are system representation in intuitive terms, and ease of development and modification. Two less-often-stated benefits are flexibility in input selection and controlled input quantization. I have addressed the first two in previous columns; the other two require some discussion.

**As powerful as rule-based representation is, the use of fuzzy logic strengthens it in a number of ways.**

*Flexibility in input selection:* For a given system design, the solution model often defines what inputs we will use. For example, in physical control systems, we work with proportional error, its integral, its derivative, and, sometimes, its second derivative. The characteristics of these inputs, their behavior in the presence of various types of noise, and how they interact with each other are all well-understood. If a system parameter or characteristic is not part of the model, we would not normally consider its possible use, and we would not know how to use it.

Working with a rule-based system makes choice of inputs an open issue. Inputs combine logically in rule conditions. Adding an input means adding it to the conditions of existing rules and creating additional rules. The choice of system parameters to use as inputs is no longer a part of the model being implemented, but rather a critical part of the design process.

*Controlled quantization:* In a rule-based system, the input space is the universe of all possible input combinations. Part of the design process is to identify those regions within the overall input space that will be active and to create rules for them. If the entire input space is valid, that is, if any combination of inputs is possible during system operation, rules must cover the entire input space.

The system designer divides the active input space into regions. A single rule governs each region. The designer typically defines each region by identifying sections of individual inputs and logically combining them. The size of each region in the overall input space is what I call its "quantization." The phrase "controlled quantization" refers to the ability to define each region size independent of the size of other regions. Its meaning also includes the ability to tighten or loosen quantization (to decrease or increase region size) easily with minimum impact to the rest of the system.

These four capabilities—system representation in intuitive terms, ease of development and modification, flexibility in input selection, and controlled input quantization—exist *not* because a system is fuzzy, but rather because rules represent its system operation. The operational model developed

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in this manner generates a response function: an output defined for collections of inputs. You can do this using if...then...rules and by other semantic techniques as well.

This conclusion is worth repeating: The four capabilities listed exist not because a system is fuzzy, but rather because it is rule-based. Concerning these four traits, the observation that opened this column is correct—sort of.

**The importance of fuzziness**

As powerful as rule-based representation is, the use of fuzzy logic strengthens it in a number of ways.

*Output interpolation:* A problem associated with crisp, rule-based systems relates to the dividing of the input space by rule conditions. As changing inputs drive the system from one input region to another, the output undergoes a discontinuous transition. This situation occurs as the rule associated with the first region stops firing and the rule associated with the second region starts firing.

**Fuzzy logic is an enabling force, increasing capabilities across many facets of existing technology.**

Decreasing the size of the input regions reduces the size and impact of these discontinuous steps; the number of rules increases as well. Alternatively, if system performance allows, filtering the output removes the higher frequency step components.

A fuzzy handling of the rule base eliminates these output discontinuities by interpolating between adjacent commanded outputs. Smooth transitions between output levels is accomplished by overlapping input regions, defining these regions with fuzzy membership functions, allowing multiple rules to simultaneously fire when inputs are in these overlapping regions, and combining the multiple actions into a single output. This is done without increasing the number of rules. In fact, through judicious use of input-function overlap, the number of rules, when compared with a crisp implementation, can actually be reduced.

*Robustness:* A second problem associated with a crisp rule base is its brittleness. The transition of inputs from a region governed by a rule to a region for which there is no rule, thereby causing system failure, is abrupt; there is no warning. The same transition in a fuzzy system is gradual, allowing for a graceful transition from being fully operational to being nonoperational. In feedback systems, this transition is especially valuable, allowing for operation to be controlled back into a controlled region.

*Linguistic variables:* Linguistic variables, implemented with fuzzy membership functions, are at the heart of Zadeh's original view of fuzzy complex systems models. Although formulated to allow modeling of extremely complex systems, linguistic variables have been the basis for designing simple and moderately complex fuzzy systems. In such systems, the use of linguistic variables is starting to give way to automatically generated variables—for example, using neural nets or genetic algorithms. However, in sparsely populated, nonoptimized, extremely complex systems, where human expertise remains a necessary part of the design process, linguistic variables will continue to be of great value.

Fuzzy logic allows not only for system operation to be expressed in fuzzy-based linguistic variables, but also for the handling of imprecise and uncertain inputs and intermediate values in a straightforward manner. Other, nonfuzzy techniques for dealing with imprecision exist, but treating such inputs as being fuzzy is easily and effectively handled.

These four traits—output interpolation, robustness, effective linguistic variables, and straightforward handling of uncertain or imprecise input—add significant power to a rule-based architecture. All are a result of using fuzzy logic.

In addition, the four traits are easily observable. There are others, but they are less tangible. By strengthening rule-based representations, fuzzy logic has allowed designers to break from previous system-modeling techniques into models that are intuitively based.

The key phrase is to "break from previous system-modeling techniques." Because using fuzzy logic for system design is new, the number of design procedures is small, and there are few cookbook approaches. The fuzzy-system designer must think through the best way of doing things rather than adapting how someone else did something similar—a situation that can only enhance the opportunity for powerful results.

One example, mentioned previously, is that the designer is free to look at nontraditional system inputs, incorporating them into rule conditions. Critics have said that Japanese consumer goods, touted as being superior because they are fuzzy, are actually superior because they use additional sensors. In general, the use of a fuzzy rule base greatly facilitates adding more sensors and taking advantage of the information they provide. Both claims—that a fuzzy system with additional sensors is more powerful only because of the fuzzy logic and that it is more powerful only because of the additional sensors—are incorrect. The power comes from a fuzzy rule base's ability to effectively use the additional sensors.

So on the surface, I agree with the opening observation: Fuzzy logic tends not to be the driving force in fuzzy-logic systems. However, we can't stop there. Well-designed fuzzy-logic systems work and work well. I see fuzzy logic not as a driving force, but as an enabling force, increasing capability across many facets of existing techniques. Its strength is subtle, yet powerful.

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*David Brubaker is a consultant in fuzzy-system design. You can reach him at Huntington Advanced Technology, 883 Santa Cruz Ave, Suite 31, Menlo Park, CA 94025-4608 or on the Internet at: brubaker@cup.portal.com.*

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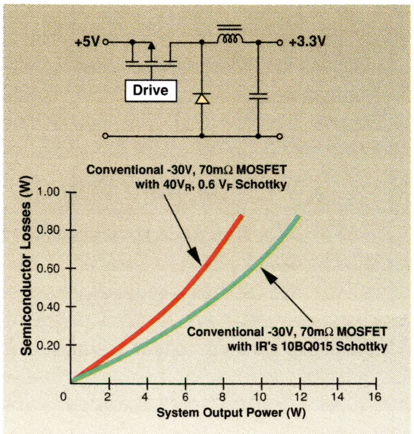

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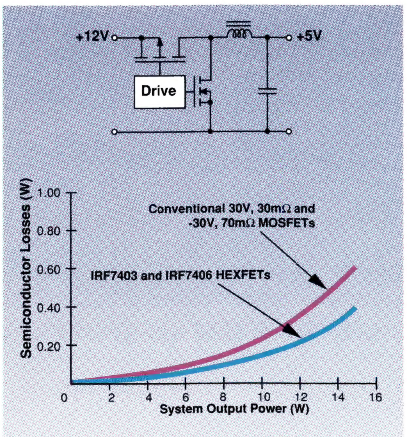

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| N-Chan. (2) | IRF7301<br>IRF7303 | 20<br>30 | 0.05<br>0.05 |
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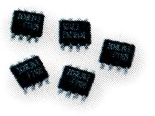

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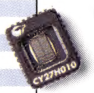

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